FLUX NC 1 PCB_98_NO_WASH

98-0002-6

TS-4300

XOPP1 NC 1 ASSEMBLY_OPTIONS

NC 1 PCB_99

99-0328-4

TS-4300-DMWX-PROTO P1	Dual Core w/ PMIC, 1GB LPDDR4x RAM, 16GB eMMC, USB-C console
TS-4300-DXWXI-PROTO P1	Dual Core w/ PMIC, 2GB LPDDR4x RAM, 32GB eMMC, USB-C console

Rev.P2 Changes needed:

- No — Remove C220 - why is it not needed?
- ✓ Change U19 to RC (delay for U23)
- ✓ Move Copper ID to Wizard - same as TS-9370
- ✓ Change iMX93 Boot Mode bit 1 to be driven by Wiz Boot_mode
- ✓ Change C43 value to 68 pF
- ✓ Change U11 pin 3 to Wiz MISO - allows Wiz only mode
- ✓ Change CN1 JTAG pins for full JTAG chain
- ✓ Change R180 and 181 to 1.8 ohm
- ✓ Change CPU ADC to match 9370_P3
- ✓ Add Res. 47K PD to ETH Reset# pins - and 47K PD on Link TMS and TDI
- ✓ Connect HC251 Copper Straps to Wiz - same as TS-9370_P2 - except Bd ID = Hex 08
- ✓ Change TDI and TDO to be non-inverted over USB Link - same as TS-9370_P3
- ✓ Change Paradigm so USB Link turns on 5V power to iMX93
- ✓ Add PU to Link_TCK and it drives Wiz_BOOT_MODE
- ✓ We want full JTAG and UART to work over USB link - same as TS-9370_P3
- ✓ Change U23 delay to turn on (5 ms) using RC (C274)
- ✓ Change Resistor straps for BOM options to be same as TS-9370_P3
- ✓ Add OR gate (U19) - so USB Link can always force power on
- ✓ Delete Wiz Reset (U20), CN88, and U88 (none are needed)
- ✓ Add TVS on Link_TCK and TMS
- ✓ Change Wizard LED3 to Yellow
- ✓ Wizard must be able to reset iMX93
- ✓ Add PD on MAX10 CONFIG_SEL
- ✓ Verify L5 decal
- ✓ Allow MIPI pairs to use CN2 LVDS diff pairs by using MUXes
- ✓ TCK can not use U29 for level shift - 3.3K PU before 1.8V rail up
- ✓ UART6 and 8 to use U28 and U29 to level shift to 1.8V
- ✓ Review all UARTs and MAX10
- ✓ I2C1 used for CN2, I2C4 to Wizard - 9370 and 9390 will change
- ✓ Add 470 ohm to GND on D13 anode
- DRAM ball size problem resolved ?
- ✓ 7 spare 470 ohm resistors - eliminate a resistor network
- ✓ Move MAX10 ball D7 off of DIO_61
- ✓ Add 100K PU to WIZ_POR#

P2 Fun Facts:

CN1 JTAG is for entire JTAG chain

CN1 pin 50 and CN2 pin 76 = SW_5.2V

I2C1 used for CN2 - I2C4 to Wizard
TS-9370/90 will be changed to match

Wiz determines Boot source for iMX93

Added Wake-up to CN2 and Wiz

BoM Option Strapping Table

0 = DNP, 1=POP

	R80	R81	R77	R78	R73	R74	R82	R75
Option 1	1	1	1	1	1	1	1	0
Option 2	1	1	1	1	1	1	0	0

POP=POPULATE

DNP=DO NOT POPULATE

P2 Problems:

Jumper wire required RN21 pin 1 to RN20 pin 4

RN21 pin 8 must be cut or lifted

Need jumper wire for SEL_LVDS to TP3
using "input only" ball on MAX10

Next Rev:

RN21-A must be removed

Add AND gate to U19 pin 2 - needed?

Add TPM IC

New WiFi radio ?

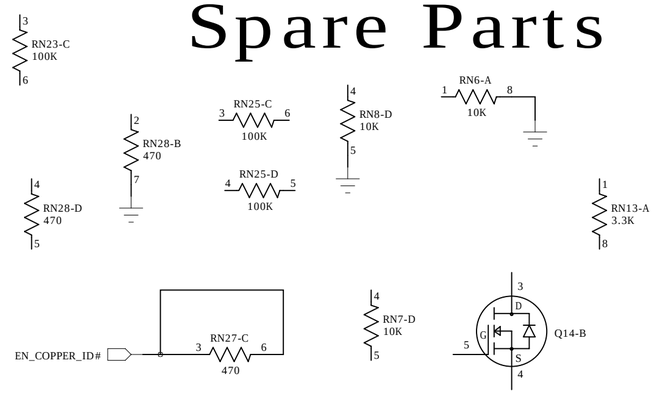
Add 3.3K across U18

Change MAX10 ball E7 to A9 - E7 is Input only

MAX10 ball B9 needs ext. 10K PU

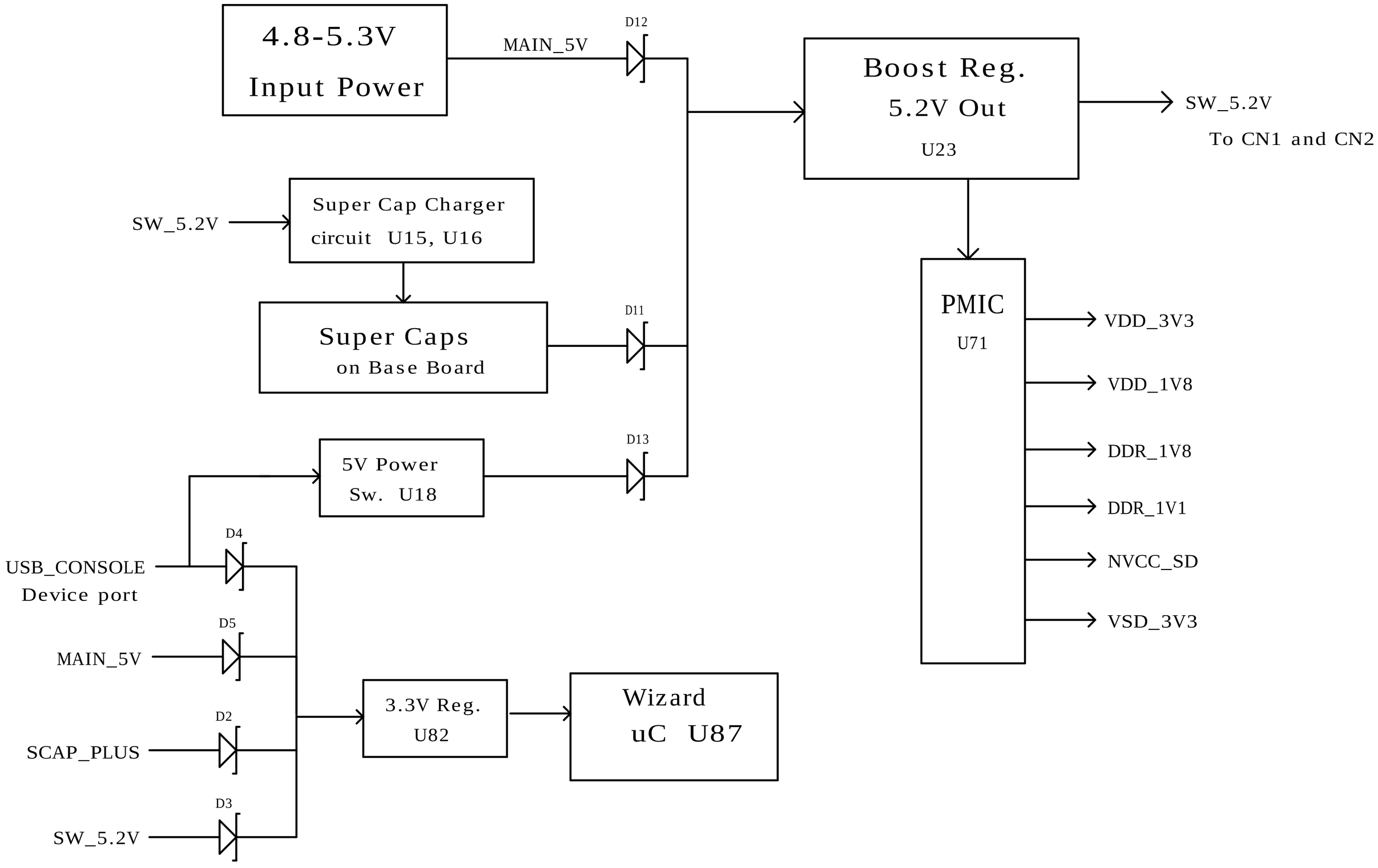
U27 pin 8 to Wiz_3.3V - R39 to 120 ohm

Spare Parts



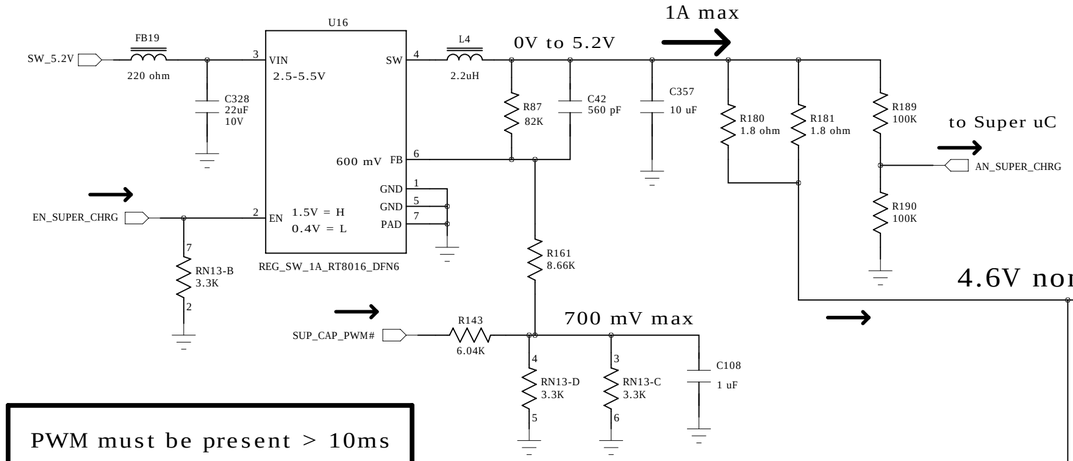
embeddedTS	Date May 7, 2025	
Title: TS-4300		
Rev: P2	Designer	Sheet 1 of 20

Power Management



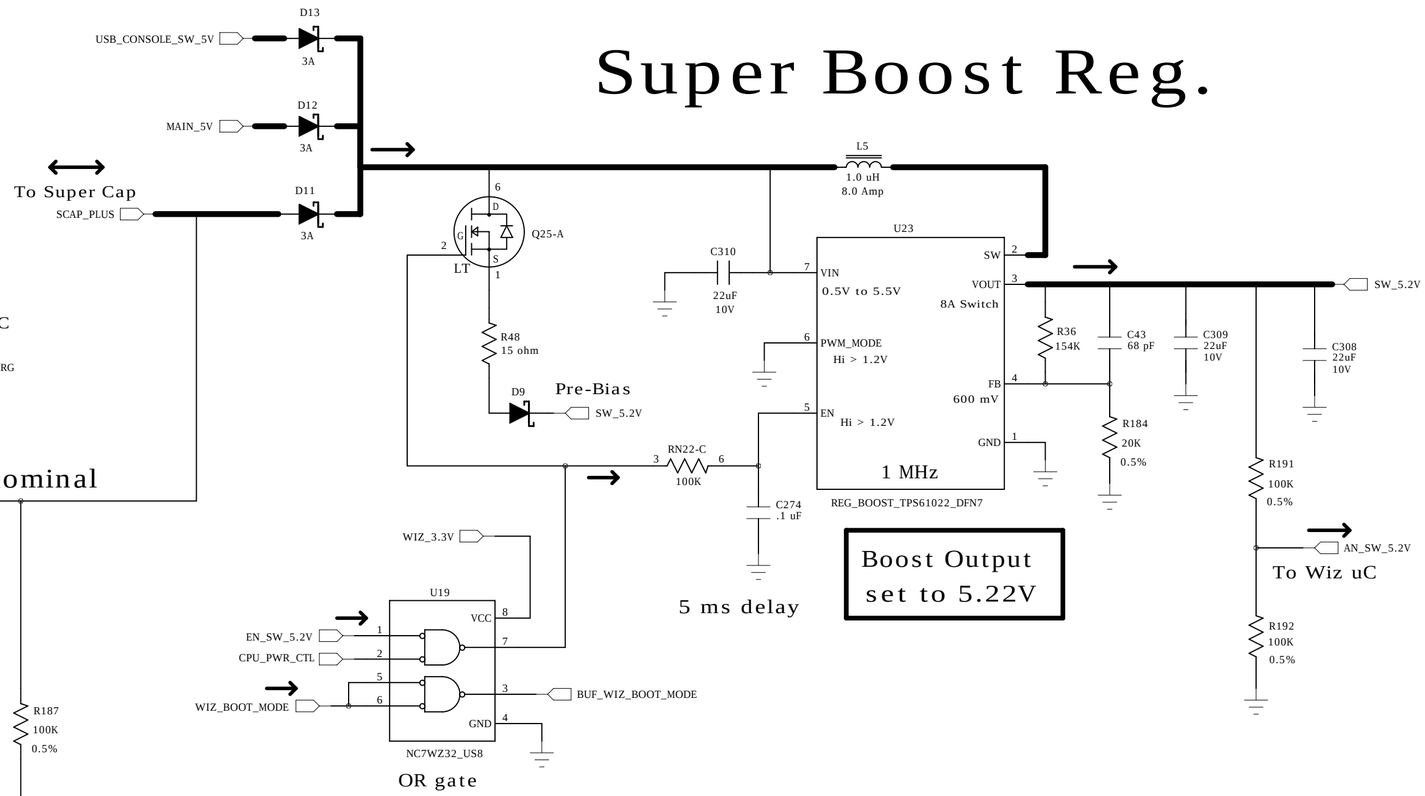
embeddedTS		Date May 7, 2025
Title: TS-4300		
Rev: P2	Designer	Sheet 2 of 20

Super Cap Charger



PWM must be present > 10ms before EN_SUPER_CHRG true

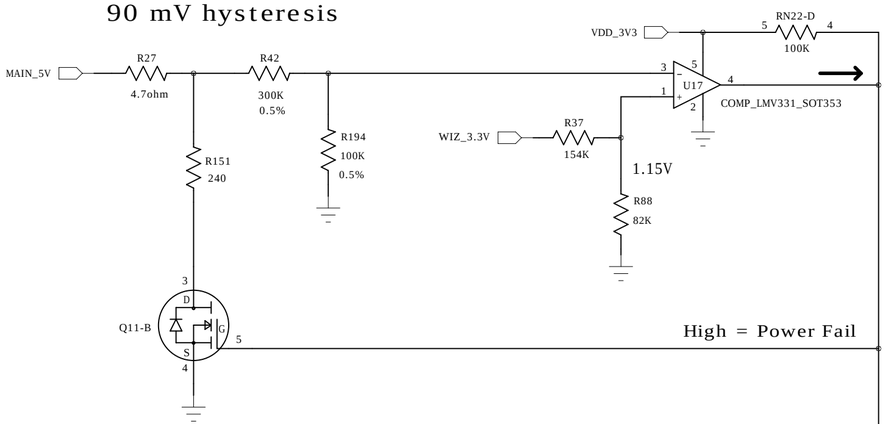
Super Boost Reg.

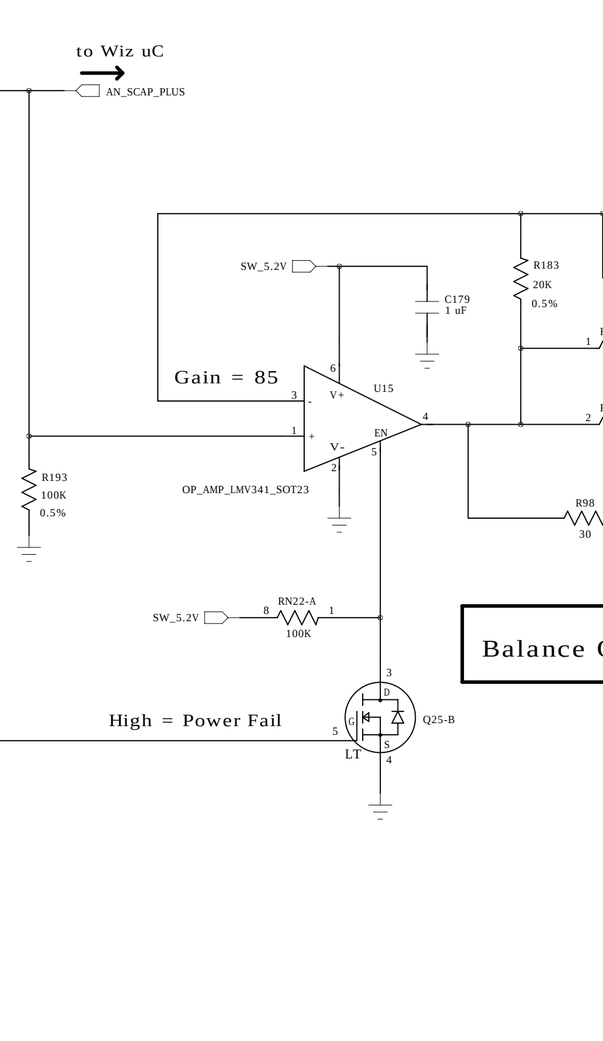


Comparitor trips at MAIN_5V = 4.59V

90 mV hysteresis

Comparator





Balance Op Amp is OFF during Discharge

Charging Rules:

Max Voltage total = 4.6V

Max Voltage on each Cap = 2.5V

Max Delta between SCap = 600 mV

embeddedTS	Date May 7, 2025	
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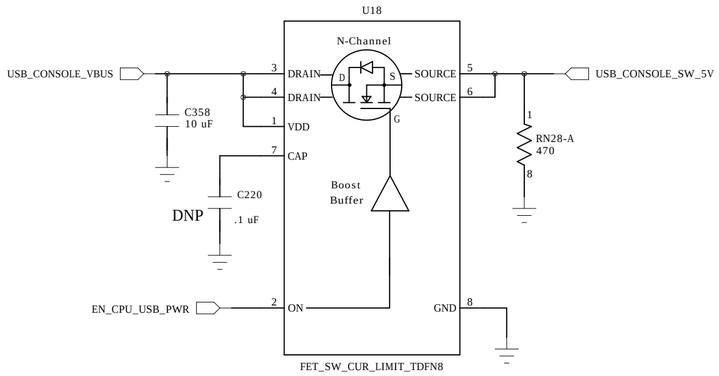
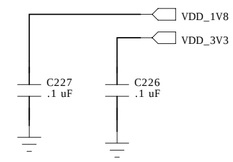
For FPGA/eMMC Programming



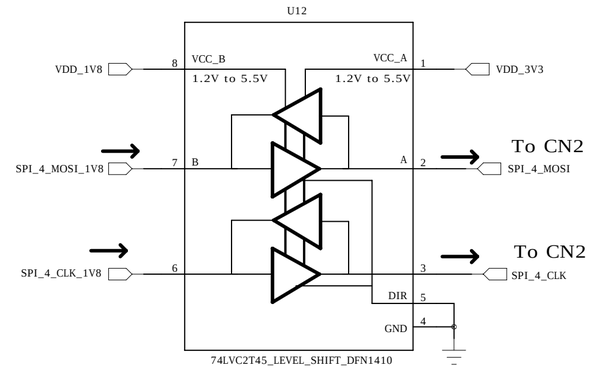
Switch enables 5V Power from Console USB when JTAG Programming eMMC and FPGA

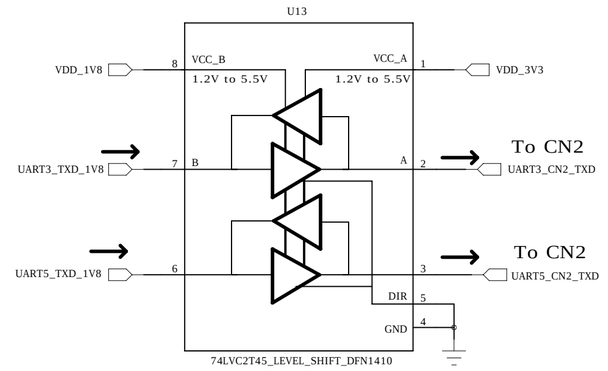


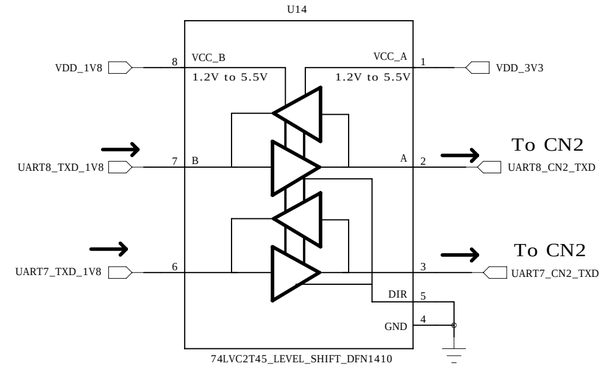
near U12 and U13

1.8V --> 3.3V

To CN2







See Sheet 17 for UART details

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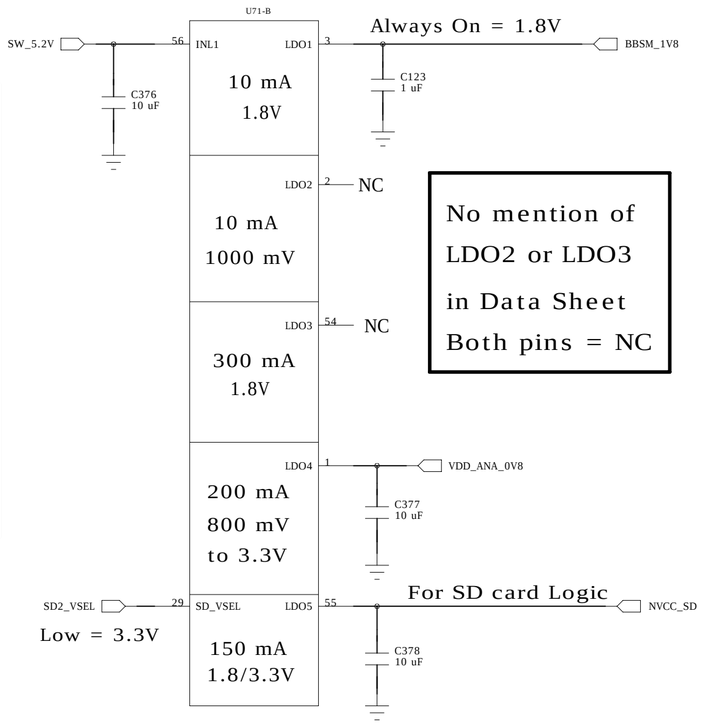
PMIC Linear Reg.



Power up Rail Seq:

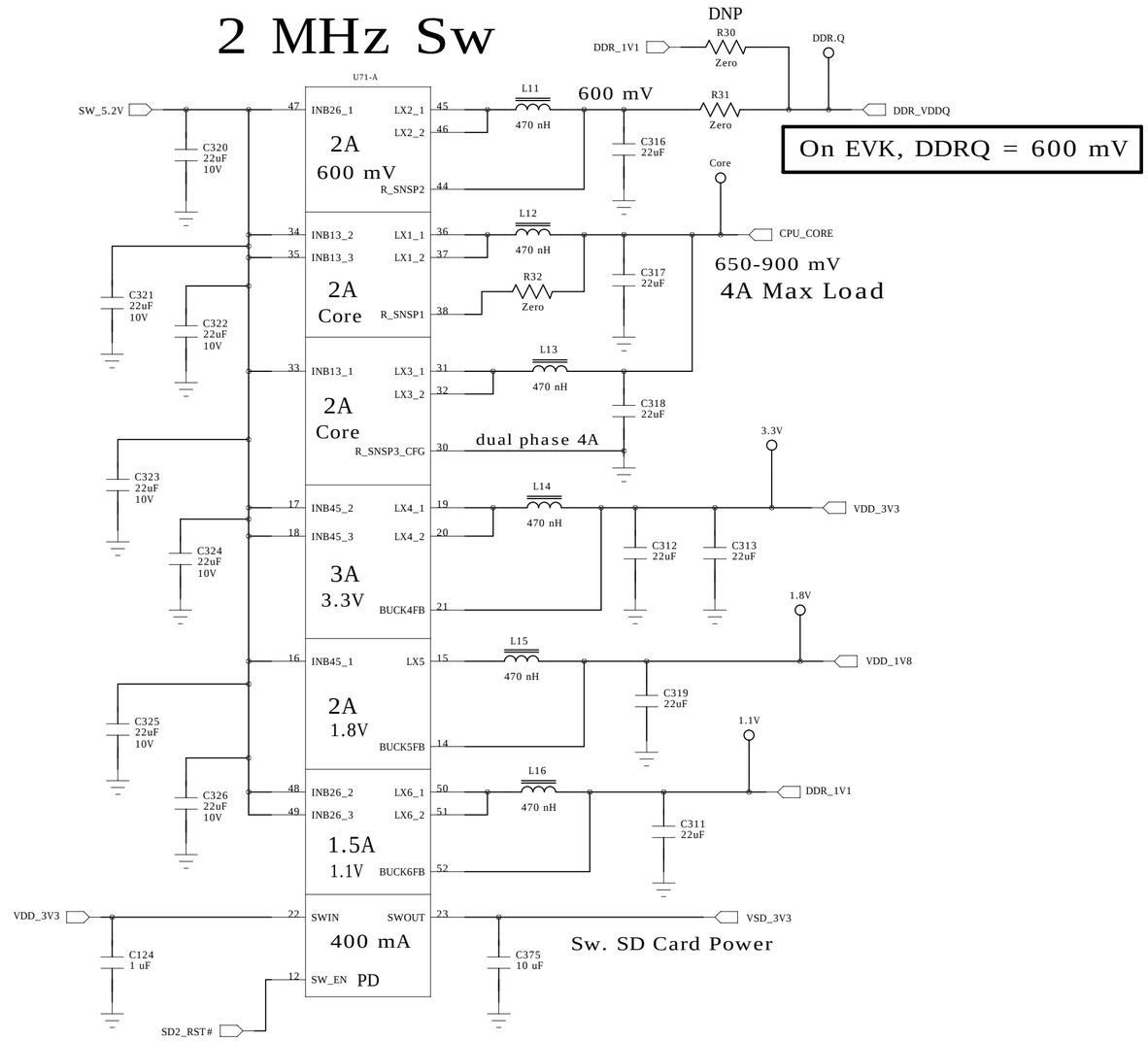
- LDO1 = Always On
- Buck_1_3 = CPU Core
- LDO4 = VDD_ANA_0V8
- Buck5 = VDD_1V8
- Buck6 = DDR_1V1
- Buck2 = DDR_VDDQ
- Buck4 = VDD_3V3
- LDO5 = NVCC_SD
- POR# deassert (20 ms)

2 ms per rail except POR#

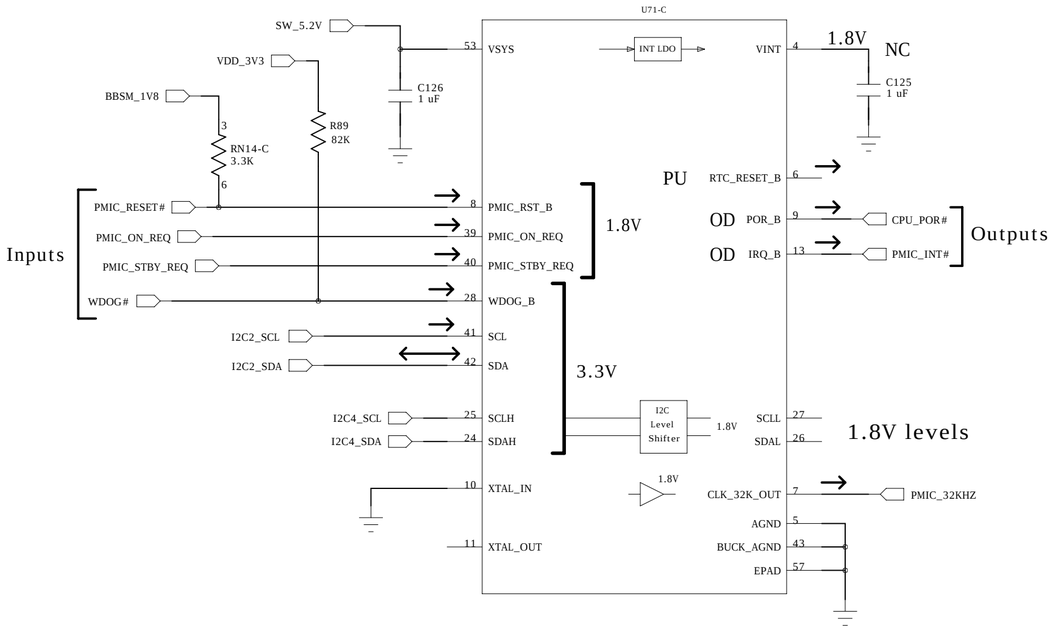
No mention of LDO2 or LDO3 in Data Sheet
Both pins = NC

PMIC Buck Reg.

2 MHz Sw



PMIC Control



POR# = Power on Reset
POR# deasserted
20 ms after all rails OK

PMIC comes out of POR @ SW_5.2V > 2.4V
plus 20 ms after all rails OK

PMIC_RST_B falling edge causes "Cold Reset"
after debounce time

Pins 5 and 43 should not be
connected directly to EPAD

If pin 10 is GND,
uses internal 32 KHz Osc.

PMIC "Cold Reset" = cycle all power rails
takes about 330 ms to complete

→ See Bob's email sent Sept 13, 2024 to Eng.

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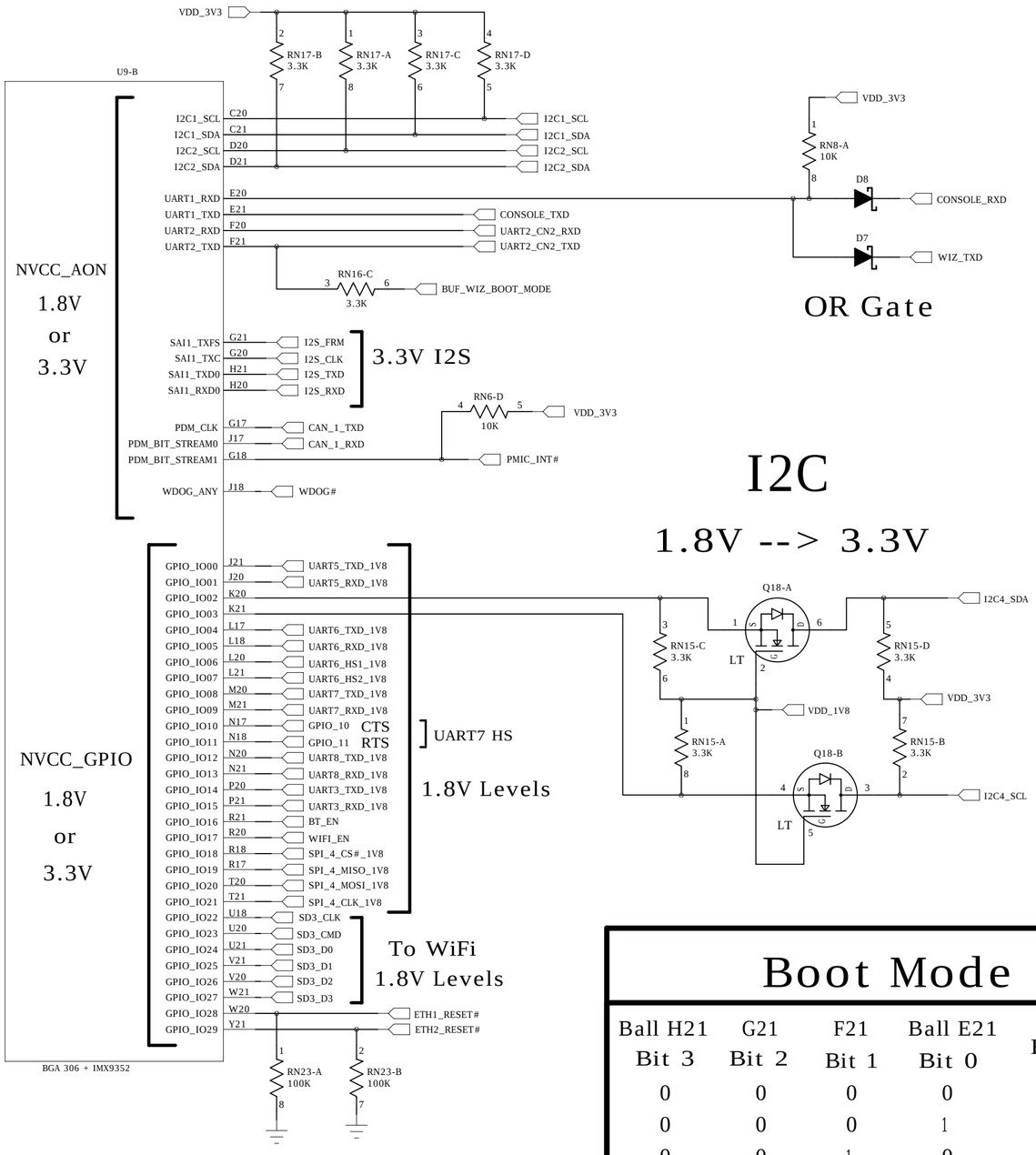
CPU GPIO



I2C

1.8V --> 3.3V

Boot Mode				
Ball H21 Bit 3	G21 Bit 2	F21 Bit 1	Ball E21 Bit 0	Boot Source
0	0	0	0	Use Fuses
0	0	0	1	USB Boot
0	0	1	0	eMMC Boot
0	0	1	1	SD Boot

Wiz Console UART RXD drives Bit 0

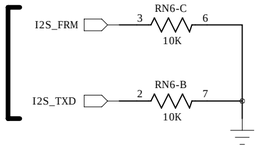
WIZ_BOOT_MODE drives Bit 1

Bits 2 and 3 are biased low

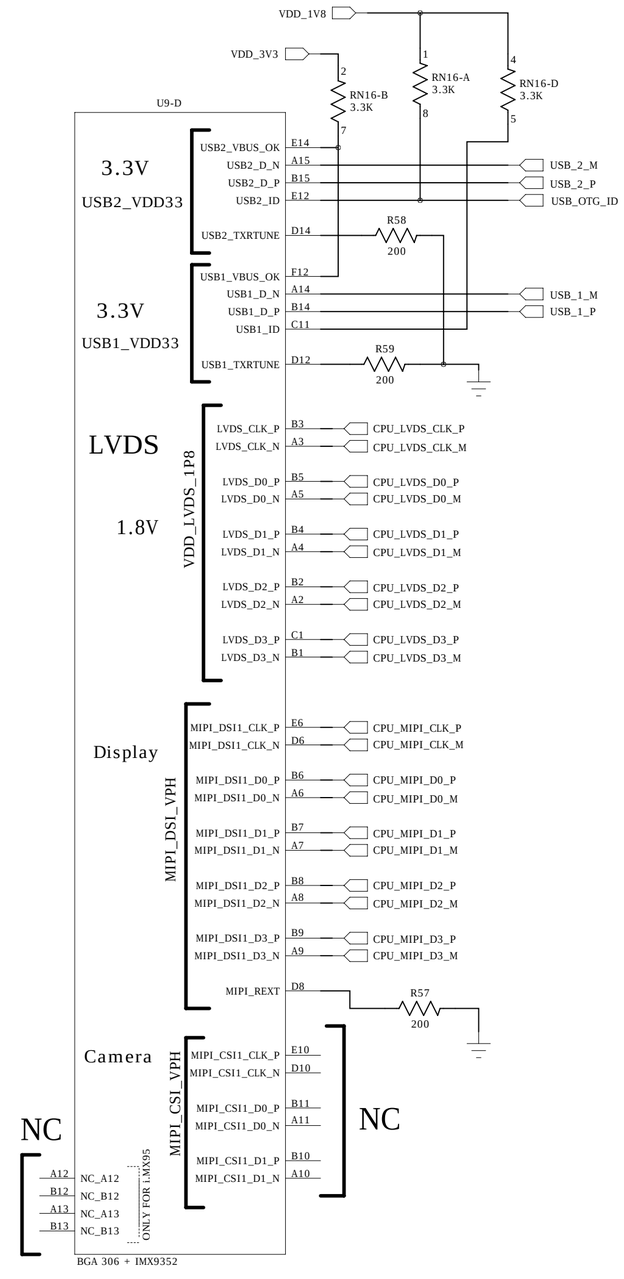
"USB Boot" refers to a USB serial downloader
--> not booting from a USB Flash drive

MS 2 bits of Boot mode is biased low
Wizard drives 2 LS bits at iMX93 reset
determines iMX93 Boot per Table

iMX93
Boot Straps
2 MS bits



CPU USB
MIPI and LVDS



R57 not needed if MIPI not used

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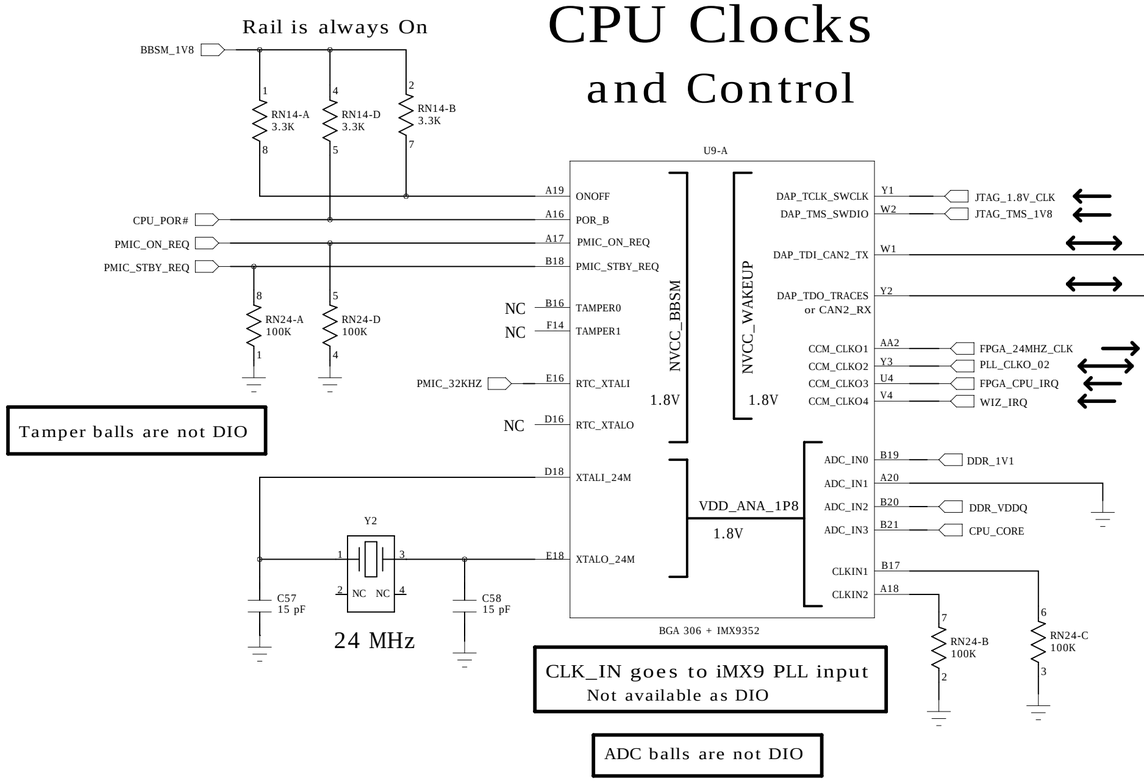
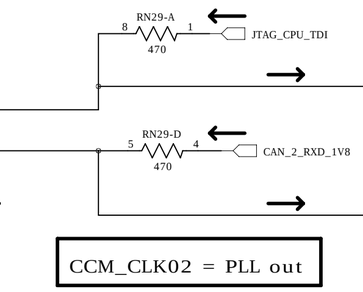
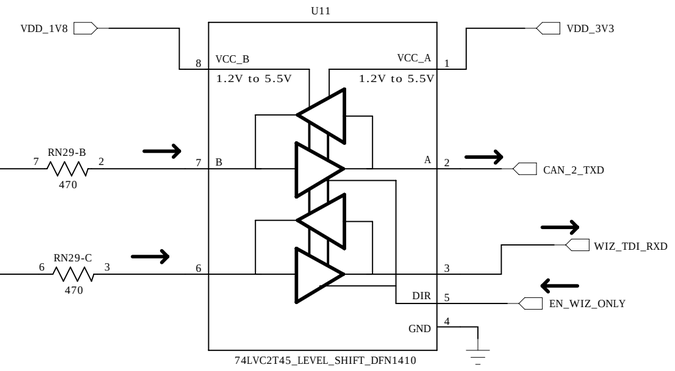
CPU Clocks and Control

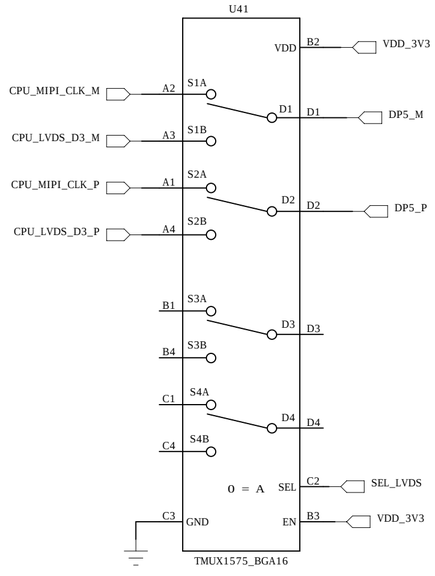


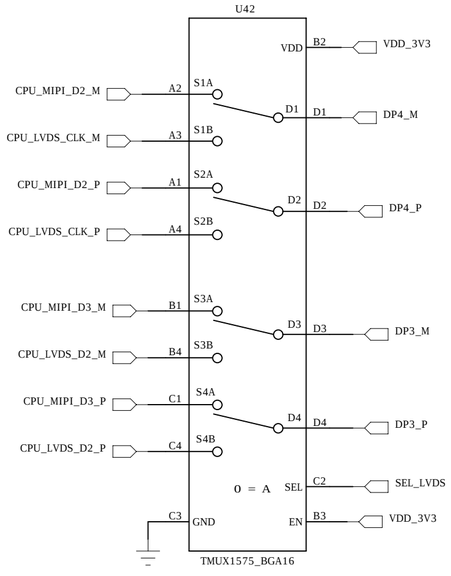


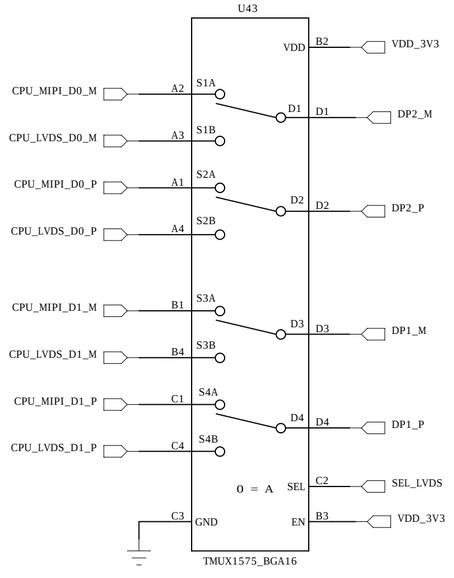
1.8V --> 3.3V



MUXes for LVDS and MIPI







Diff Pairs Length (mm)

	LVDS	MIPI
DP1	D1 = 54.8	D1 = 57.9
DP2	D0 = 54.0	D0 = 55.3
DP3	D2 = 53.8	D3 = 59.8
DP4	CLK = 53.8	D2 = 59.5
DP5	D3 = 54.0	CLK = 66.3

embeddedTS	Date May 7, 2025	
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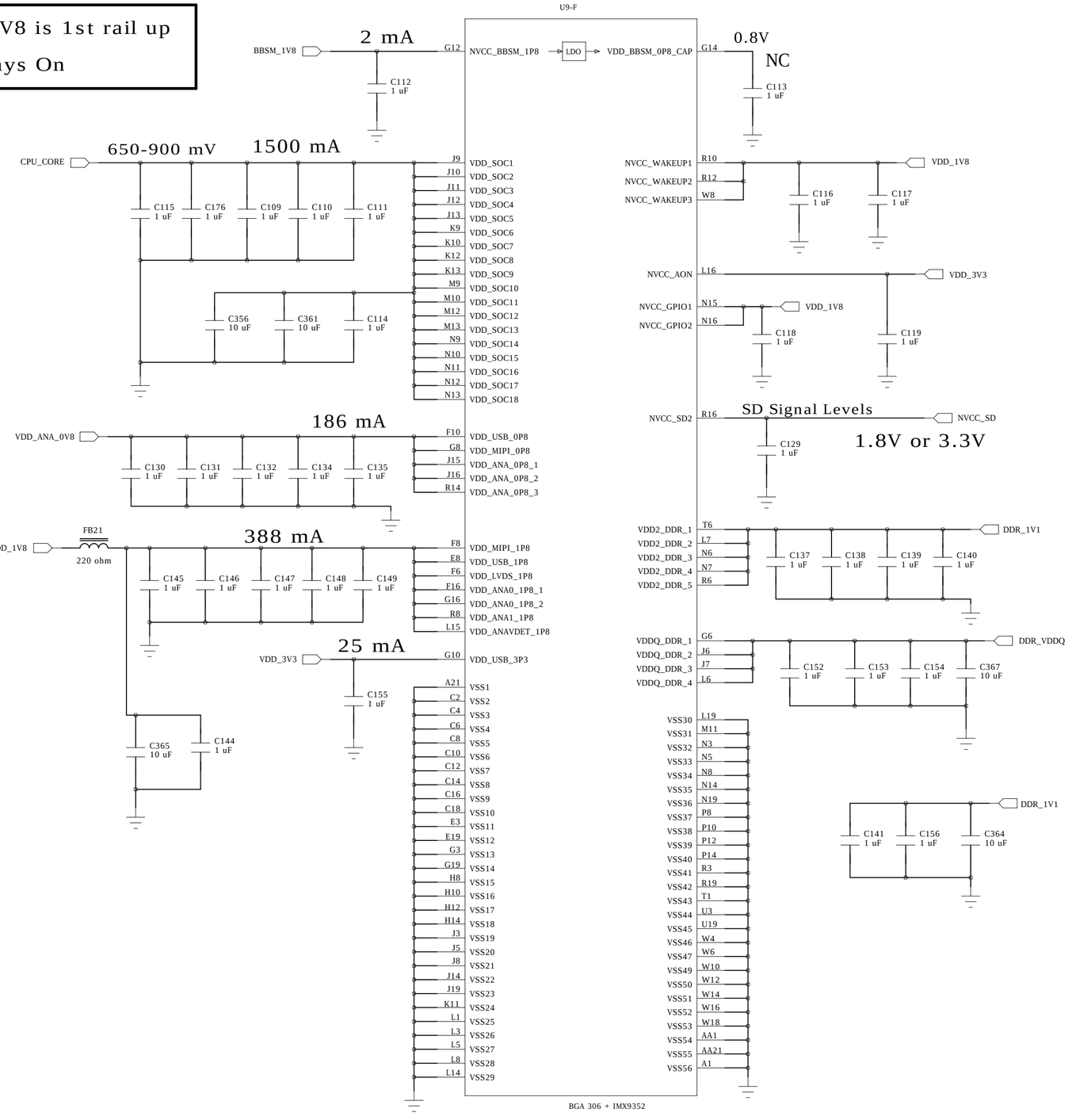
CPU Power

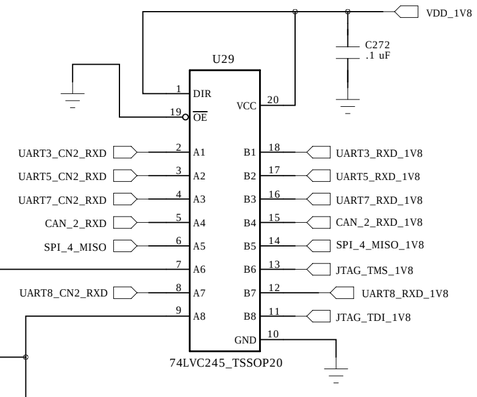
At Power up, BBSM_1V8 is 1st rail up
this rail is always On

1.8V NVCC_WAKEUP = ENET, SD1, SD3, JTAG
3.3V NVCC_AON = UART, I2C, I2S, CAN1, WDOG
NVCC_GPIO = GPIO 00 thru 29 - EVK = 3.3V

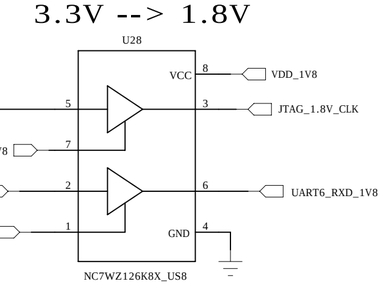


Level Shifters

3.3V --> 1.8V



JTAG
To CN1
and CN4



3.3V --> 1.8V

JTAG Chain
3.3V levels

LINK_TCK can not use U29
bc it has PU to WIZ_3.3V
before VDD_1V8 rail is up

when VCC = 0
Inputs are Hi-Z

Inputs are 7V tolerant
at any VCC

embeddedTS	Date May 7, 2025	
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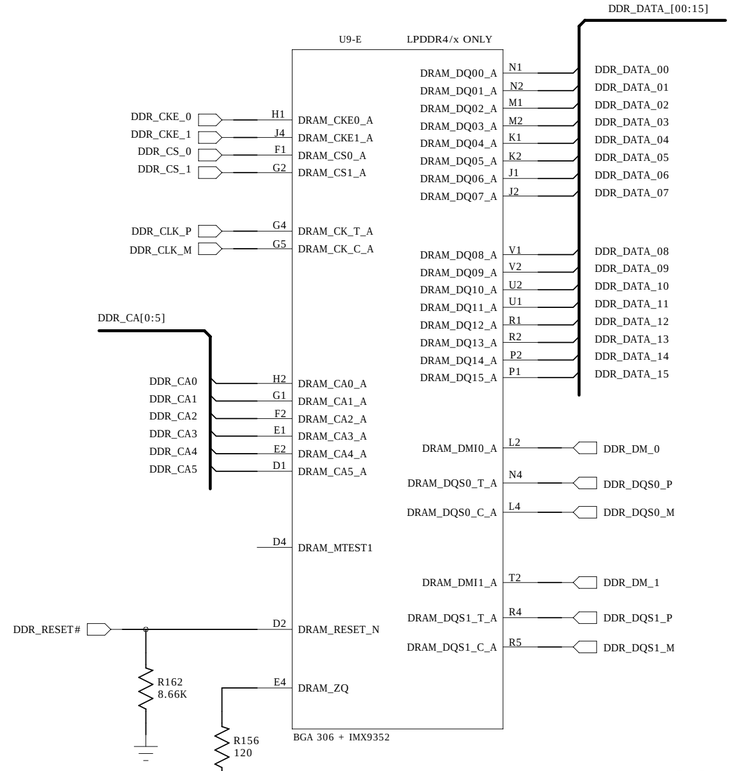
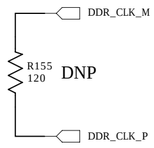
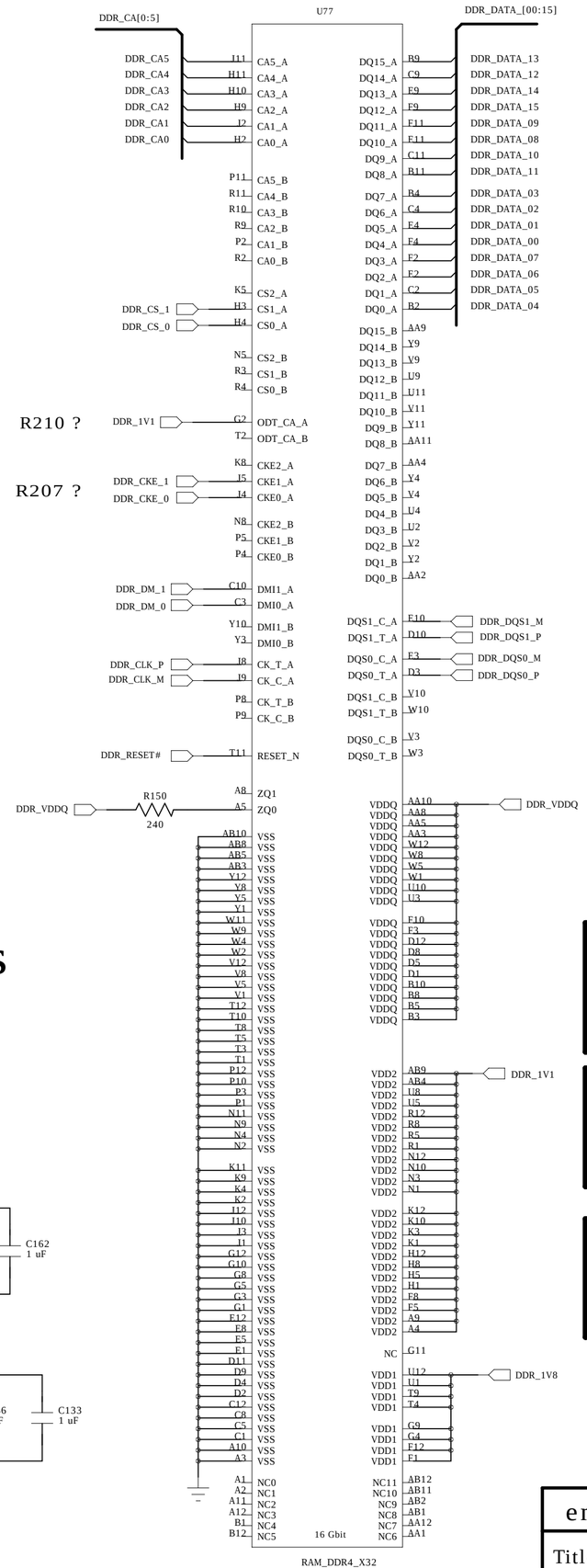
iMX93 RAM Interface



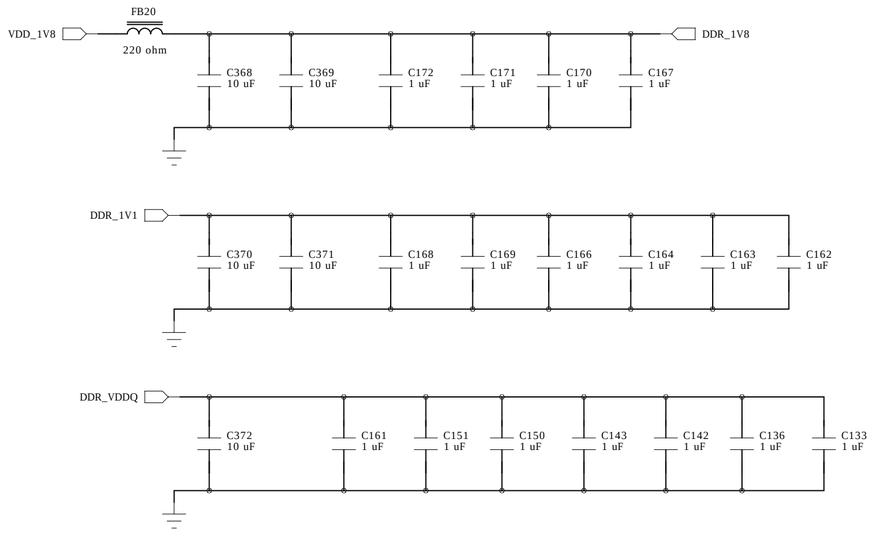
2 GB Max DDR Address space



LPDDR4 RAM



LPDDR4 Bypass Caps



On EVK, DDRQ = 600 mV

Micron FW package
requires 0.4mm pad size
16 Gbit samples use this
8 Git samples require .35 pad

EVK had 0.35 mm pads for RAM
But used RAM that needs 0.4

We are using exact same
Micron 16 Gbit RAM as EVK

DDR_1.8V rail must always
be greater than other rails

Current on 1.8V rail
estimated to be <100 mA

Current on other 2 rails
about 800 mA max. per RAM

embeddedTS	Date May 7, 2025	
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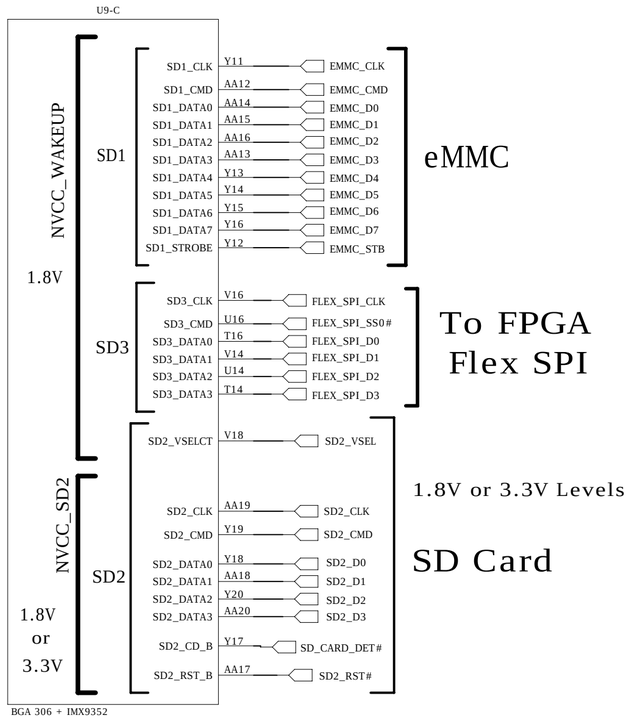
iMX93

SD1 SD2 SD3 interfaces

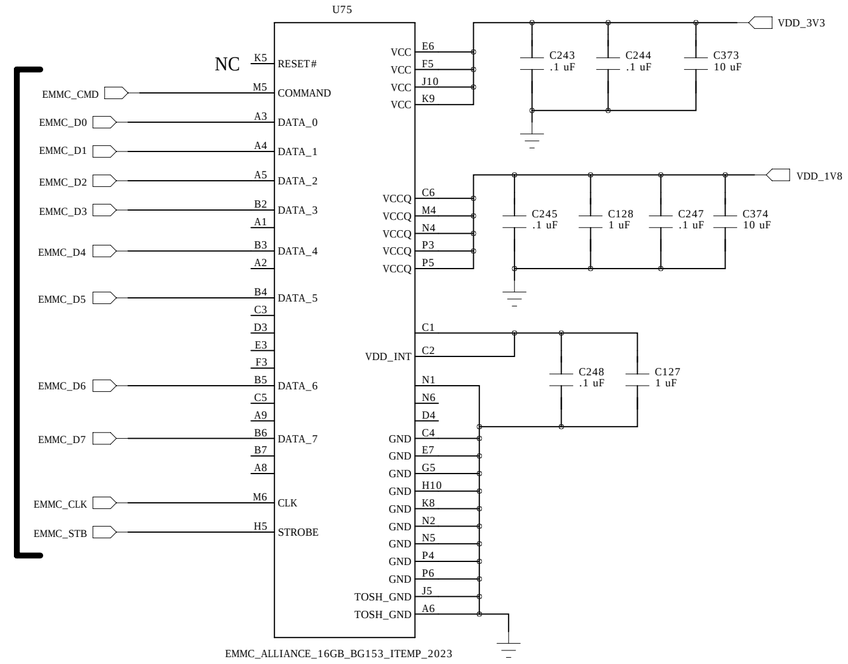


Flash Memory

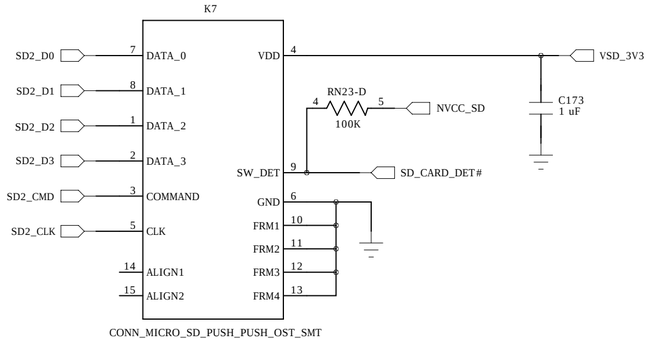
eMMC 16 GByte

eMMC
1.8V Levels

Requires matched traces
all 50 ohm impedance
within 2.5 mm

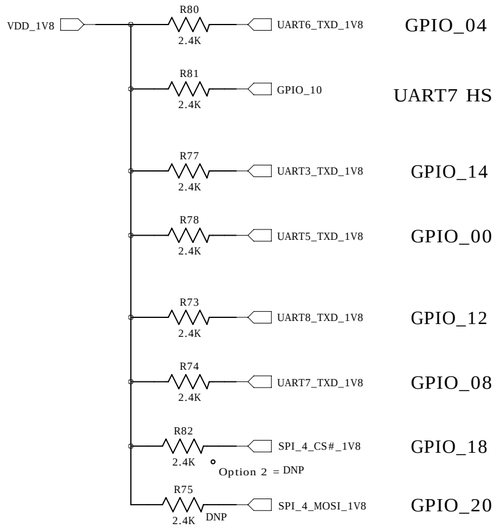


Push-Push
SD Card Socket



signal lines can use 1.8V or 3.3V levels
But power is always Sw. 3.3V
NVCC_SD = 1.8 or 3.3V

BOM Option Straps



Same straps as TS-9370

Rev. P1 TEMPORARY Strapping Options

Configuration	R80
4300-DMWXI-PROTO	POPULATED
4300-DXWXI-PROTO	NOT POPULATED

*temporary strapping option for P1 boards ONLY

4300-DX = 2GB RAM, 32GB eMMC
4300-DM = 1GB RAM, 16GB eMMC

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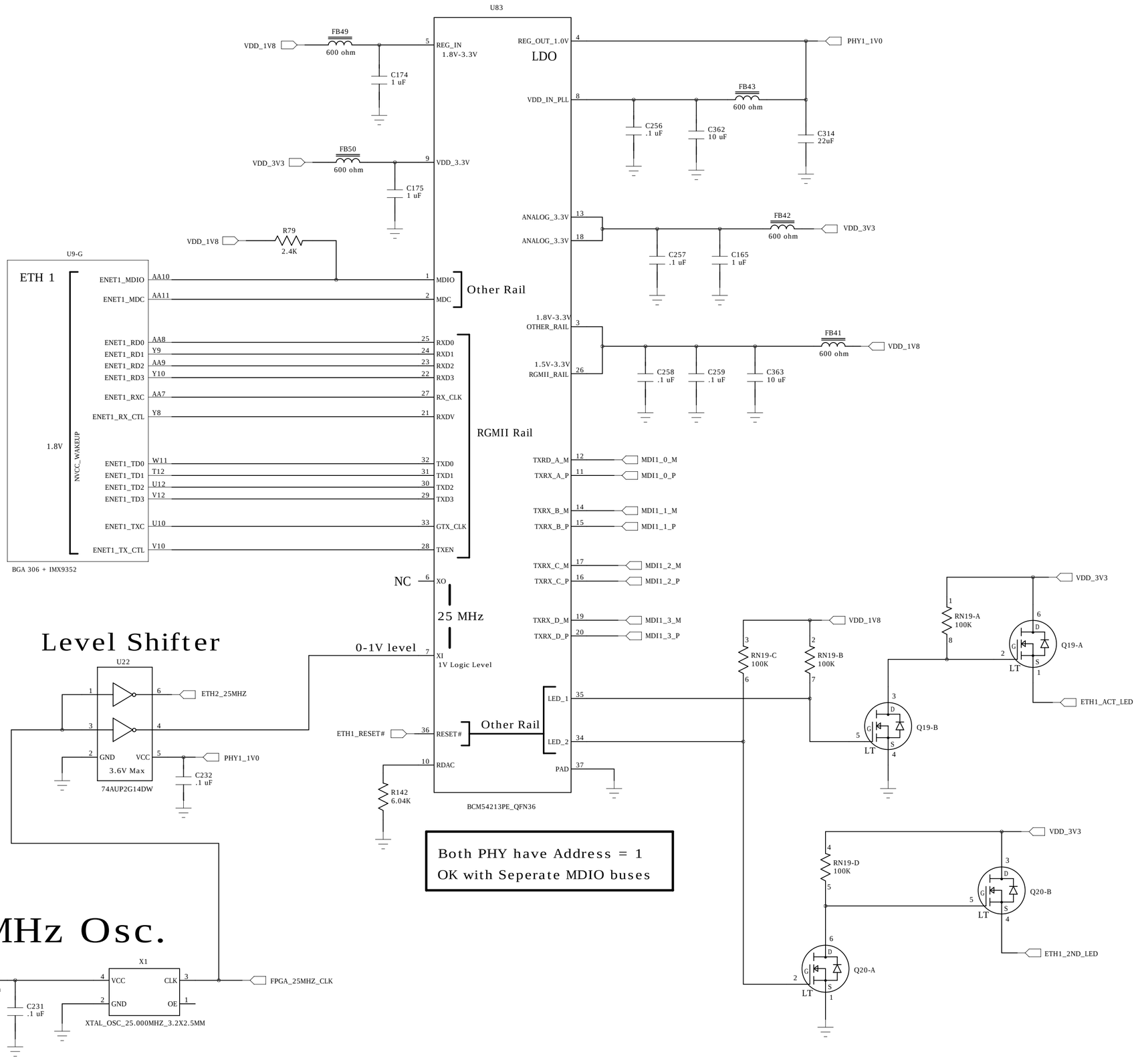
10/100/1000 Ethernet PHY 1



embeddedTS	Date May 7, 2025	
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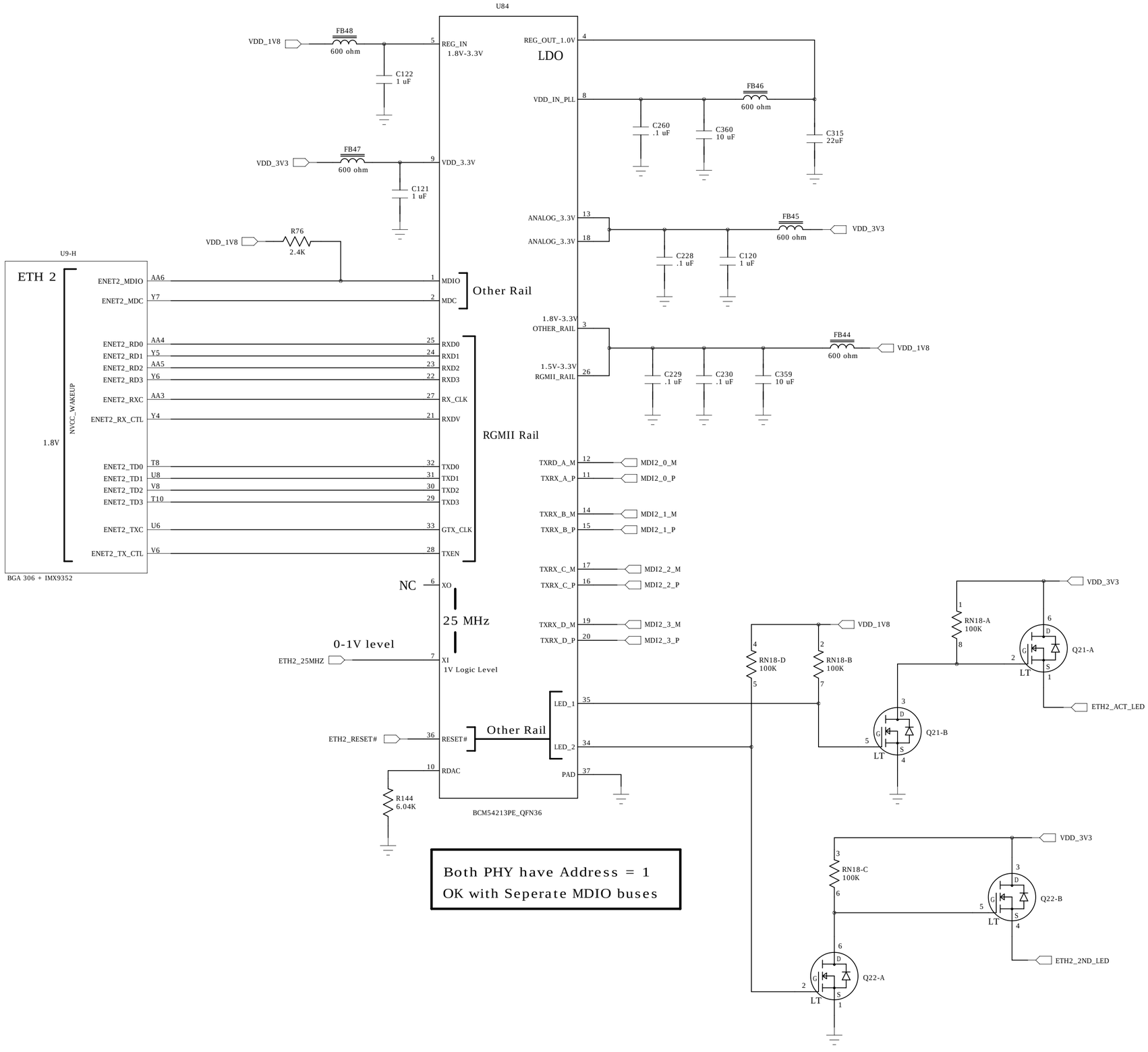
10/100/1000 Ethernet PHY 2



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Rev: P2	Designer	Sheet 12 of 20

MAX10 FPGA

126 DIO + JTAG

108 DIO + 4 Special

14 DIO + JTAG

U10-B

3.3V DIO

Enable PU on Unused balls

DIO_[00:99]

DIO_01	B2	IO_8_B2/DIFFIO_RX_T26N	IO_2_N2/DPCLK0/DIFFIO_RX_L22N	N2	DIO_57
DIO_02	B3	IO_8_B3/DIFFIO_RX_T23P	IO_2_M3/PLL_L_CLKOUTN/DIFFIO_RX_L27N	M3	DIO_58
DIO_03	A2	IO_8_A2/DIFFIO_RX_T26P	IO_2_N3/DPCLK1/DIFFIO_RX_L22P	N3	DIO_59
DIO_04	A3	IO_8_A3/DIFFIO_RX_T21N	IO_8_C9/DIFFIO_RX_T14N	C9	DIO_60
DIO_05	A6	IO_8_A6/DIFFIO_RX_T19N	IO_6_F8/DIFFIO_RX_R27P	F8	DIO_61
DIO_06	B5	IO_8_B5/DIFFIO_RX_T20N	IO_8_D8/DEV_OE/DIFFIO_RX_T18P	D8	DIO_62
DIO_07	A8	IO_8_A8/DIFFIO_RX_T15P	IO_6_D9/DIFFIO_RX_R31N	D9	DIO_63
DIO_08	B10	IO_8_B10/DIFFIO_RX_T16P	CLK1N__BANK2_DIFFIO_RX_L20N	H5	DIO_64
DIO_09	D11	IO_6_D11/DIFFIO_RX_R33N	IO_3_K6/DIFFIO_TX_RX_B7P	K6	DIO_65
DIO_10	B11	IO_6_B11/DIFFIO_RX_R28N	IO_3_K7/DIFFIO_TX_RX_B9P	K7	DIO_66
DIO_11	C11	IO_6_C11/DIFFIO_RX_R29N	IO_3_J6/DIFFIO_TX_RX_B7N	J6	DIO_67
DIO_12	C12	IO_6_C12/DIFFIO_RX_R29P	CLK0P__BANK2_DIFFIO_RX_L18P	H6	DIO_68
DIO_13	B12	IO_6_B12/DIFFIO_RX_R28P	IO_6_E10/DIFFIO_RX_R31P	E10	DIO_69
DIO_14	C13	IO_6_C13	IO_6_E9/DIFFIO_RX_R27N	E9	DIO_70
DIO_15	H4	CLK1P__BANK2_DIFFIO_RX_L20P	IO_5_K11/DIFFIO_RX_R2P	K11	DIO_71
DIO_16	J1	IO_2_J1/DIFFIO_RX_L19N	IO_6_F10/DPCLK2/DIFFIO_RX_R26N	F10	DIO_72
DIO_17	J2	IO_2_J2/DIFFIO_RX_L19P	IO_8_E8/DIFFIO_RX_T18N	E8	DIO_73
DIO_18	K1	IO_2_K1/DIFFIO_RX_L28N	IO_3_J7/DIFFIO_TX_RX_B9N	J7	DIO_74
DIO_19	K2	IO_2_K2/DIFFIO_RX_L28P	IO_8_A11/DIFFIO_RX_T17N	A11	DIO_75
DIO_20	L1	VREF_BANK2_HI_CAP	IO_5_H8/DIFFIO_RX_R10N	H8	DIO_76
DIO_21	L3	IO_2_L3/PLL_L_CLKOUTP/DIFFIO_RX_L27P	IO_5_H9/DIFFIO_RX_R10P	H9	DIO_77
DIO_22	L4	IO_3_L4/DIFFIO_TX_RX_B1P	IO_3_J8/DIFFIO_TX_RX_B14N	J8	DIO_78
DIO_23	J5	IO_3_J5/DIFFIO_TX_RX_B3P	IO_5_J9/DIFFIO_RX_R8P	J9	DIO_79
DIO_24	L5	IO_3_L5/DIFFIO_TX_RX_B1N	IO_3_L10/DIFFIO_TX_RX_B16P	L10	DIO_80
DIO_25	K5	IO_3_K5/DIFFIO_TX_RX_B3N	IO_5_J10/DIFFIO_RX_R1N	J10	DIO_81
DIO_26	M4	IO_3_M4/DIFFIO_RX_B2N	IO_5_K10/DIFFIO_RX_R1P	K10	DIO_82
DIO_27	N4	IO_3_N4/DIFFIO_RX_B4N	IO_3_L11/DIFFIO_TX_RX_B12P	L11	DIO_83
DIO_28	M5	IO_3_M5/DIFFIO_RX_B2P	IO_5_H10/DIFFIO_RX_R8N	H10	DIO_84
DIO_29	G13	IO_5_G13/DIFFIO_RX_R11P	CLK2N__BANK6_DIFFIO_RX_R14N	G10	DIO_85
DIO_30	N5	IO_3_N5/DIFFIO_RX_B4P	CLK2P__BANK6_DIFFIO_RX_R14P	G9	DIO_86
DIO_31	N6	IO_3_N6/DIFFIO_TX_RX_B5N	VREF_BANK5_HI_CAP	K13	DIO_87
DIO_32	M7	IO_3_M7/DIFFIO_TX_RX_B5P	IO_6_F9/DPCLK3/DIFFIO_RX_R26P	F9	DIO_88
DIO_33	N7	IO_3_N7/DIFFIO_RX_B6N	IO_5_H13/DIFFIO_RX_R9N	H13	DIO_89
DIO_34	K8	IO_3_K8/DIFFIO_TX_RX_B14P	IO_5_G12/DIFFIO_RX_R11N	G12	DIO_90
DIO_35	N8	IO_3_N8/DIFFIO_RX_B6P	IO_8_A4/DIFFIO_RX_T21P	A4	
DIO_36	M8	IO_3_M8/DIFFIO_RX_B8N	IO_8_D7/CONFIG_SEL	D7	
DIO_37	N9	IO_3_N9/DIFFIO_RX_B11P	IO_5_J13/DIFFIO_RX_R9P	J13	POWER_FAIL#
DIO_38	M9	IO_3_M9/DIFFIO_RX_B8P	IO_8_B6/DIFFIO_RX_T20P	B6	
DIO_39	N10	IO_3_N10/DIFFIO_RX_B11N	IO_8_D6/CRC_ERROR/DIFFIO_RX_T22N	D6	EN_LS_UART6_RXD
DIO_40	M10	IO_3_M10/DIFFIO_TX_RX_B16N	IO_8_B4/DIFFIO_RX_T23N	B4	SPI4_CN2_CS#
DIO_41	N11	VREF_BANK3_HI_CAP	IO_8_A7/DIFFIO_RX_T19P	A7	TP4
DIO_42	M11	IO_3_M11/DIFFIO_TX_RX_B12N	IO_6_A12/DIFFIO_RX_R30N	A12	UART6_CN2_RXD
DIO_43	N12	IO_3_N12	IO_8_A10/DIFFIO_RX_T17P	A10	UART6_CN2_TXD
DIO_44	M12	IO_3_M12/DIFFIO_TX_RX_B10P	IO_8_A9/DIFFIO_RX_T15N	A9	TP3
DIO_45	M13	IO_3_M13/DIFFIO_TX_RX_B10N	IO_8_A5	A5	
DIO_46	L12	IO_5_L12/DIFFIO_RX_R2N	IO_8_C10/DIFFIO_RX_T14P	C10	EN_USB_HOST_5V
DIO_47	L13	IO_5_L13	IO_6_B13/DIFFIO_RX_R30P	B13	PMIC_RESET#
DIO_48	K12	IO_5_K12/DIFFIO_RX_R7P	IO_6_D12/DIFFIO_RX_R33P	D12	EN_GREEN_LED#
DIO_49	J12	IO_5_J12/DIFFIO_RX_R7N	VREF_BANK6_HI_CAP	D13	EN_RED_LED#
DIO_50	F12	IO_6_F12/DIFFIO_RX_R18P	VREF_BANK8_HI_CAP	B7	
DIO_51	F13	CLK3P__BANK6_DIFFIO_RX_R16P	CLK0N__BANK2_DIFFIO_RX_L18N	G5	
DIO_52	E12	IO_6_E12/DIFFIO_RX_R18N			
DIO_53	E13	CLK3N__BANK6_DIFFIO_RX_R16N			
DIO_54	L2	IO_2_L2			
DIO_55	M1	IO_2_M1/DIFFIO_RX_L21N			

DIO_[00:99]

DIO_08 is EXT_RESET# on TS-8551 and 4100

it must be able to drive PMIC_RESET#

DIO_79 must be capable of being TXEN for UART2

KorralKool needs it

CN1 pin 57 (DIO_74) must offer PWM - for TS-4100 compatibility

KorralKool needs it

VDD_3V3 — RN21-A 100K (8 / 1) — CPU_PWR_CTL

CPU_PWR_CTL requires jumper wire

Config_Sel must be biased low

R160 8.66K

UART6_CN2_RXD and TXD must be capable of connecting to UART7 HS lines

Also must allow both to be Inputs to CPU

Both must be interrupts for KorralKool

PMIC_RESET# must act like Open Drain i.e it can drive low only

LEDs

VDD_3V3 — RN7-A 10K (1/8), RN7-B 10K (2/7), RN7-C 10K (3/6) — Done, Status, Config

These 3 balls must have PU resistors at power up

OFF_BD_RESET#

SEL_LVDS

CPU_POR_3V# ← needs PU

REG_RESET# = ball B9 must be used as Reset# (input)

Special Bank 8 Balls

IO_8_C5/CONF_DONE/DIFFIO_RX_T24N	C5	
IO_8_C4/NSTATUS/DIFFIO_RX_T24P	C4	OFF_BD_RESET#
INPUT_ONLY_BANK8_NO_PU__NCONFIG	E7	SEL_LVDS
IO_8__REG_RESET#__DIFFIO_RX_T16N	B9	CPU_POR_3V#

must be NC — D3 ADC_VREF_ONLY, D2 ANALOG_IN_ONLY — ADC

GND unused ADC Inputs

FPGA_MAX10_13X13_4300

U10-C

Bank 1 = 1.8V

Enable PU on Unused balls

Flex Bus From CPU

FLEX_SPI_CLK	B1	IO_1A_B1/ADC11IN6/DIFFIO_RX_L5P
FLEX_SPI_SS0#	C2	IO_1A_C2/ADC11IN2/DIFFIO_RX_L1P
FLEX_SPI_D0	D1	IO_1A_D1/ADC11IN1/DIFFIO_RX_L1N
FLEX_SPI_D1	E3	IO_1A_E3/ADC11IN3/DIFFIO_RX_L3N
FLEX_SPI_D2	C1	IO_1A_C1/ADC11IN5/DIFFIO_RX_L5N
FLEX_SPI_D3	E4	IO_1A_E4/ADC11IN4/DIFFIO_RX_L3P
FPGA_25MHZ_CLK →	F1	IO_1A_F1/ADC11IN7/DIFFIO_RX_L7N
FPGA_24MHZ_CLK →	F4	IO_1B_F4/DIFFIO_RX_L14N
PLL_CLKO_02 ↔	H3	IO_1B_H3/DIFFIO_RX_L16P
FPGA_CPU_IRQ ←	E5	IO_1B_E5__JTAGEN
UART6_TXD_1V8 →	E1	IO_1A_E1/ADC11IN8/DIFFIO_RX_L7P
SPI_4_CS#_1V8 →	H1	VREF_BANK1_HI_CAP

UART7 HS

GPIO_10	G4	IO_1B_G4/DIFFIO_RX_L14P
GPIO_11	H2	IO_1B_H2/DIFFIO_RX_L16N

JTAG

JTAG_TDI_1V8 →	F5	IO_1B_JTAG_TDI
JTAG_1.8V_CLK →	G2	IO_1B_JTAG_TCK
JTAG_TMS_1V8 →	G1	IO_1B_JTAG_TMS
JTAG_CPU_TDI ←	F6	IO_1B_JTAG_TDO

If JTAG > 2.5V levels need ext. clamp diodes

FPGA_MAX10_13X13_4300

PLL_CLK0_02 can be interrupt to CPU

UART7 HS can be TXEN for UART2 ?

Can FPGA_24MHZ be TXEN for UART2 ?

if BlueTooth not being used iMX93 UART6 can be repurposed and used with CN2 pins 98 and 100

No UART needed in MAX10 for first product release

But must add UART to MAX10 fabric if want to use both CN2 pins 98/100 and BT

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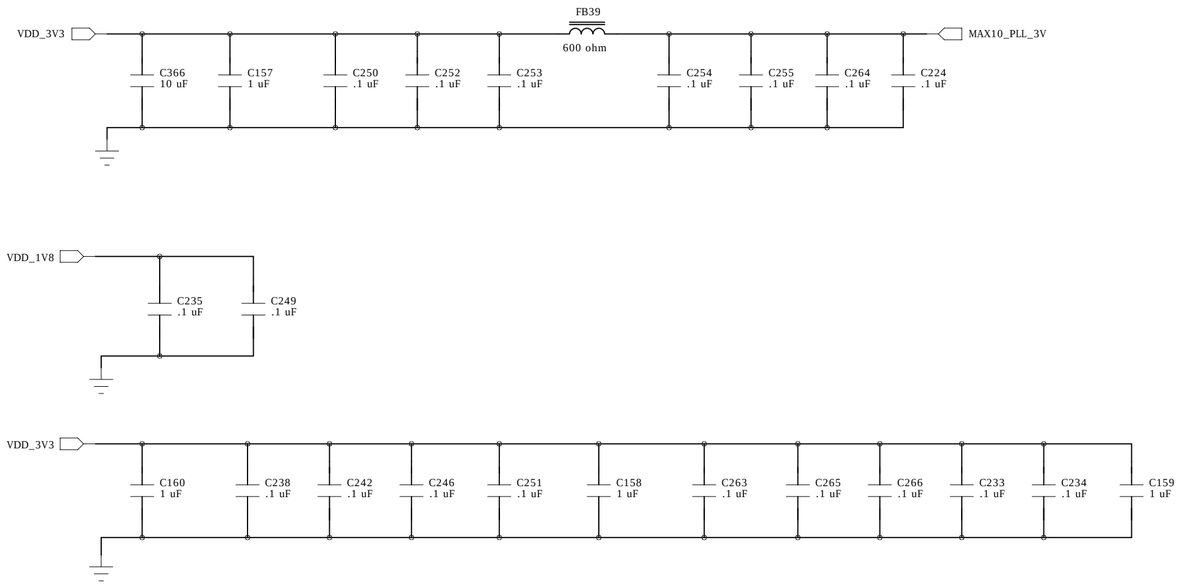
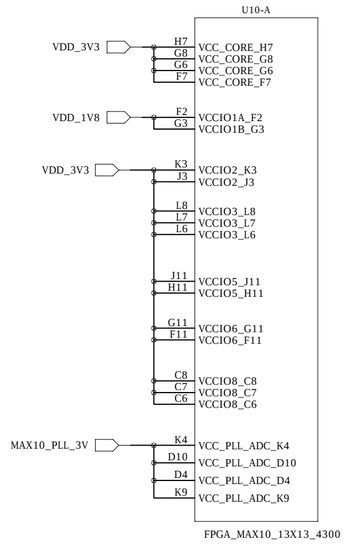
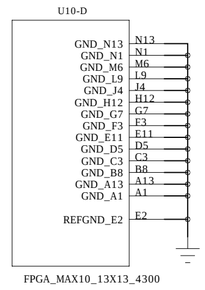
FPGA Bypass Caps



FPGA Power Rails

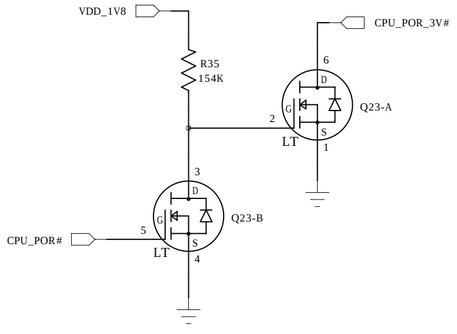


FPGA GND Balls



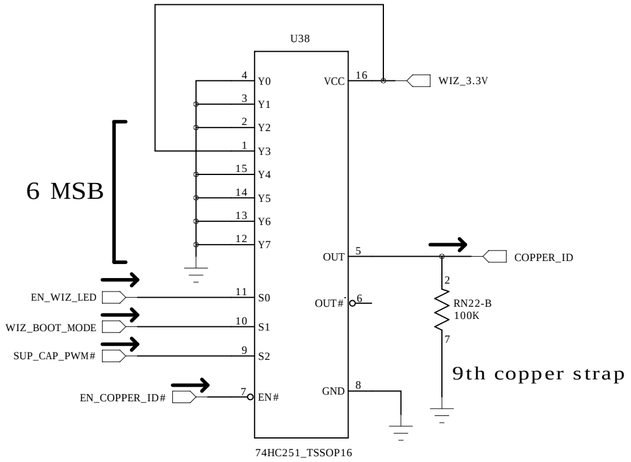
MAX10 Reset

1.8V --> 3.3V
Level Shifter



9 Copper Straps

Board ID = Hex 08



6 MSB = product ID
2 LSB + 9th bit
= Bd. revision

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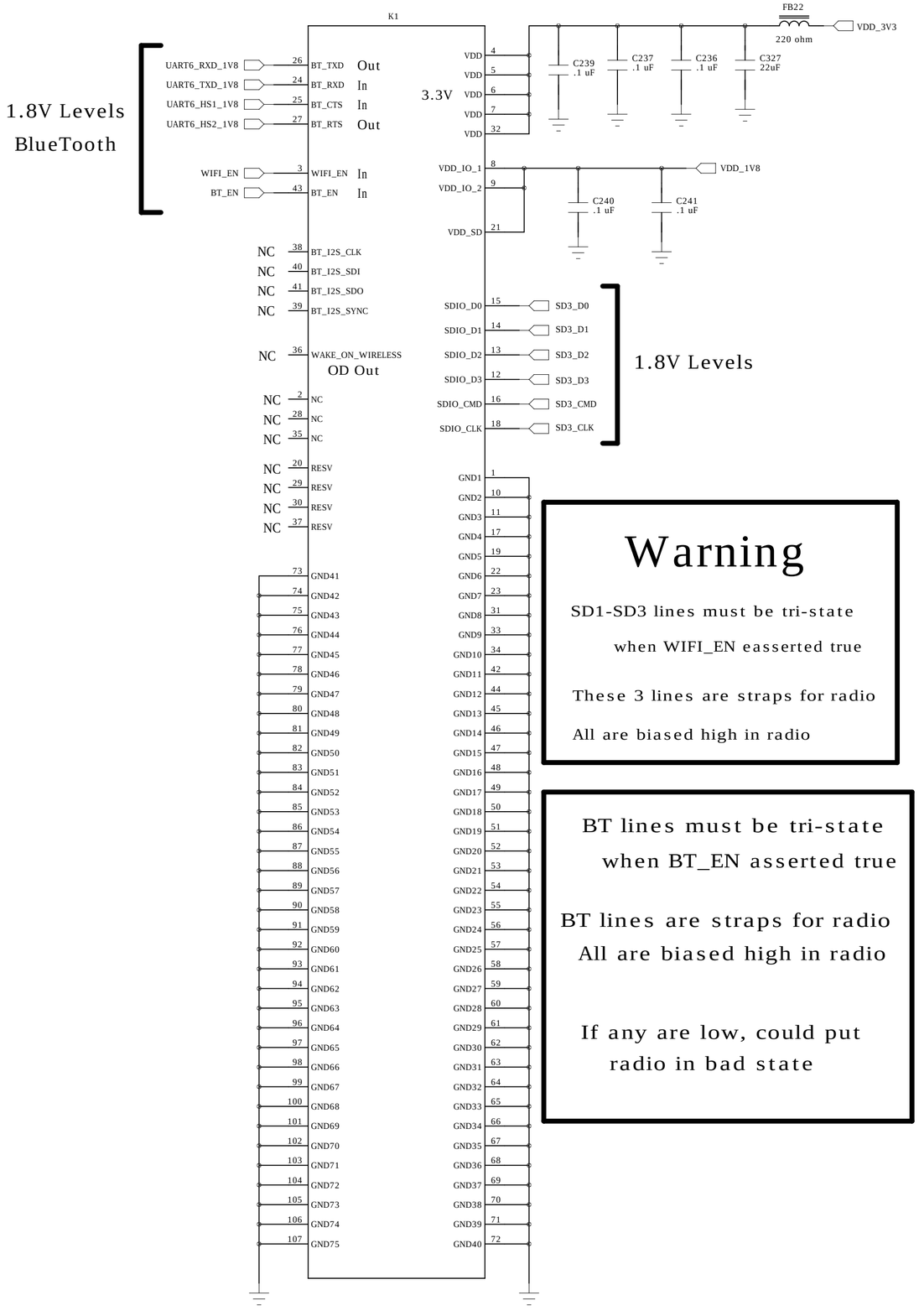
Silex WiFi Radio



Warning

SD1-SD3 lines must be tri-state
when WIFI_EN easserted true

These 3 lines are straps for radio
All are biased high in radio

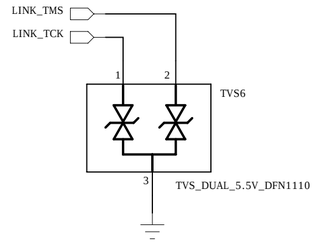
BT lines must be tri-state
when BT_EN asserted true

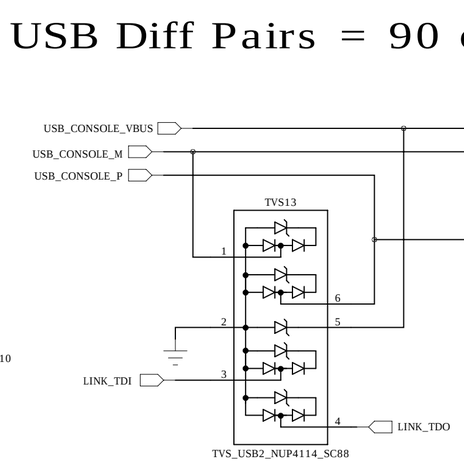
BT lines are straps for radio
All are biased high in radio

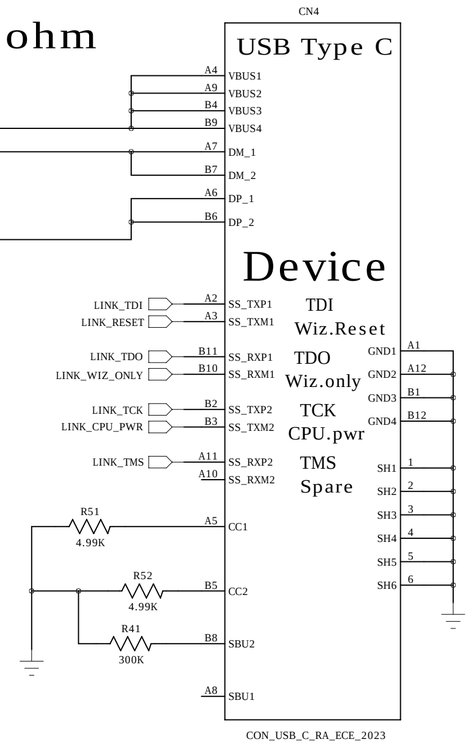
If any are low, could put
radio in bad state

USB Console

USB Diff Pairs = 90 ohm







USB Link Control Lines

In USB cable:

A2 connected to B11 A3 connected to B10	twisted pair
B11 connected to A2 B10 connected to A3	twisted pair
B2 connected to A11 B3 connected to A10	twisted pair
A11 connected to B2 A10 connected to B3	twisted pair

Also see Page 343 of USB Spec.

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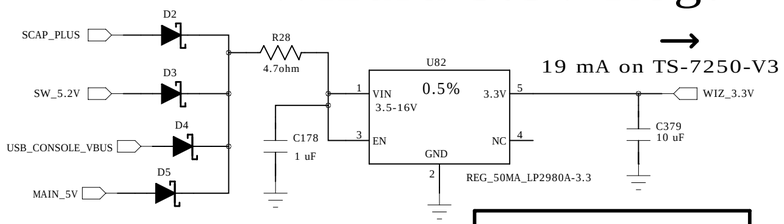
Wizard 3.3V Reg.

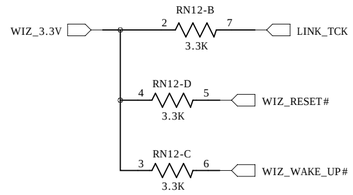


D5 needed for low-power Sleep and at start up

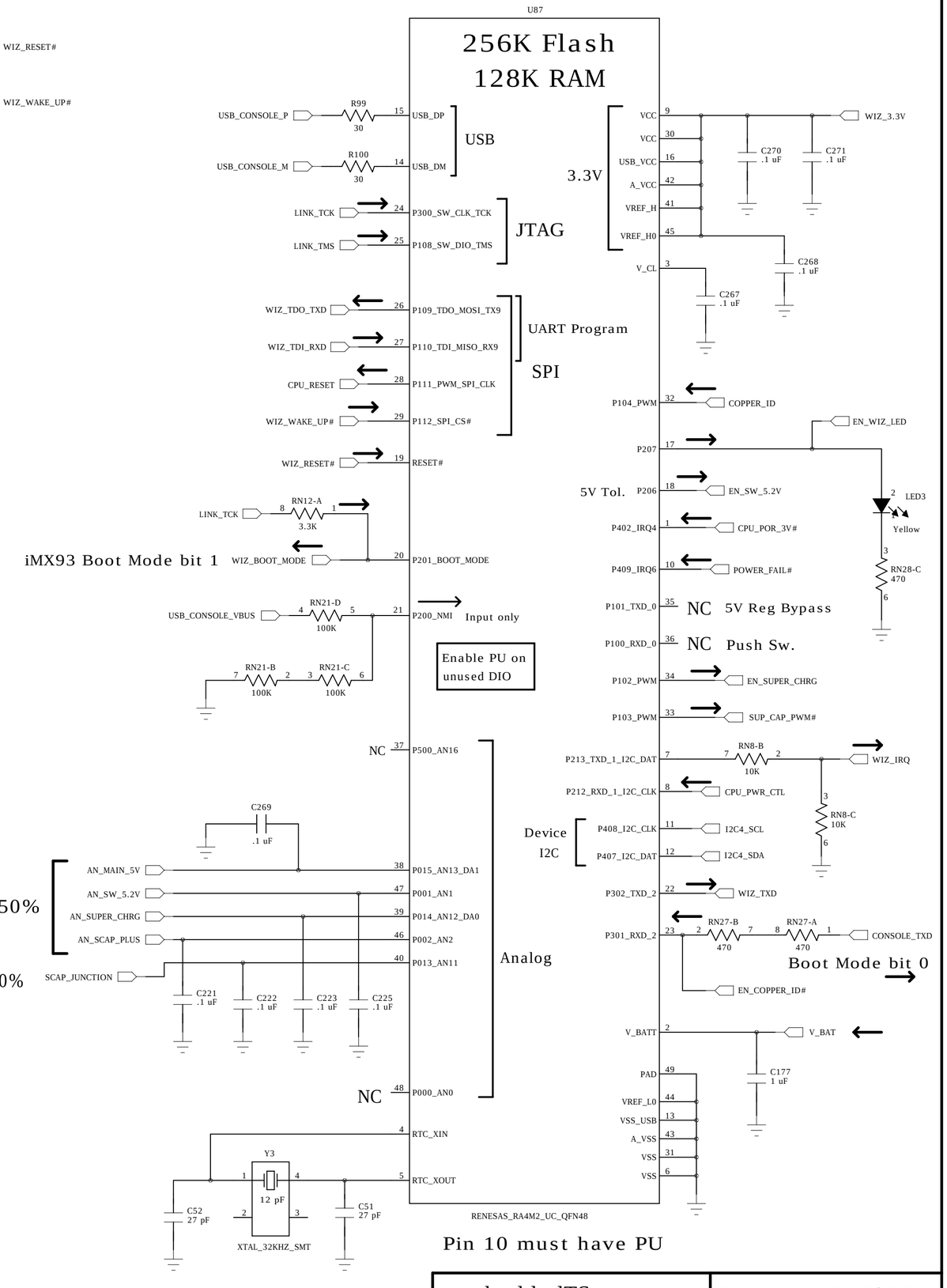
R28 prevents ringing from USB hot plug

D2 needed when SW_5.2V is off

10uF must have 30+ mohm
7mm of 6 mil trace = 36

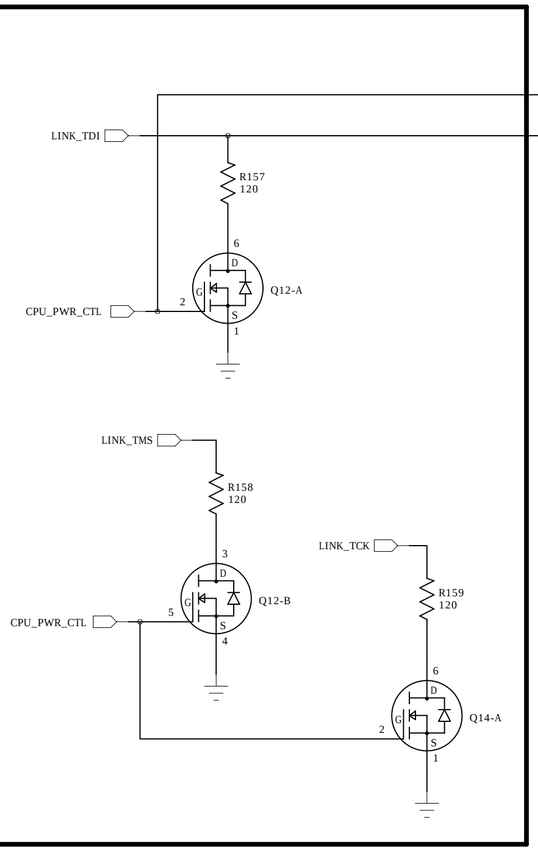


Wizard uC

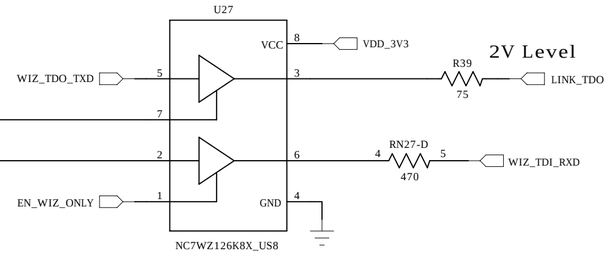


Pin 10 must have PU

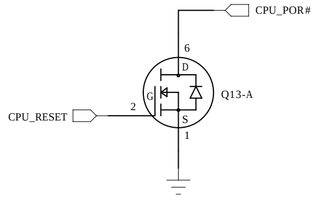
Link Term. Resistors



Wizard Drivers



iMX93 Reset



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Two 100-pin Off-board Connectors

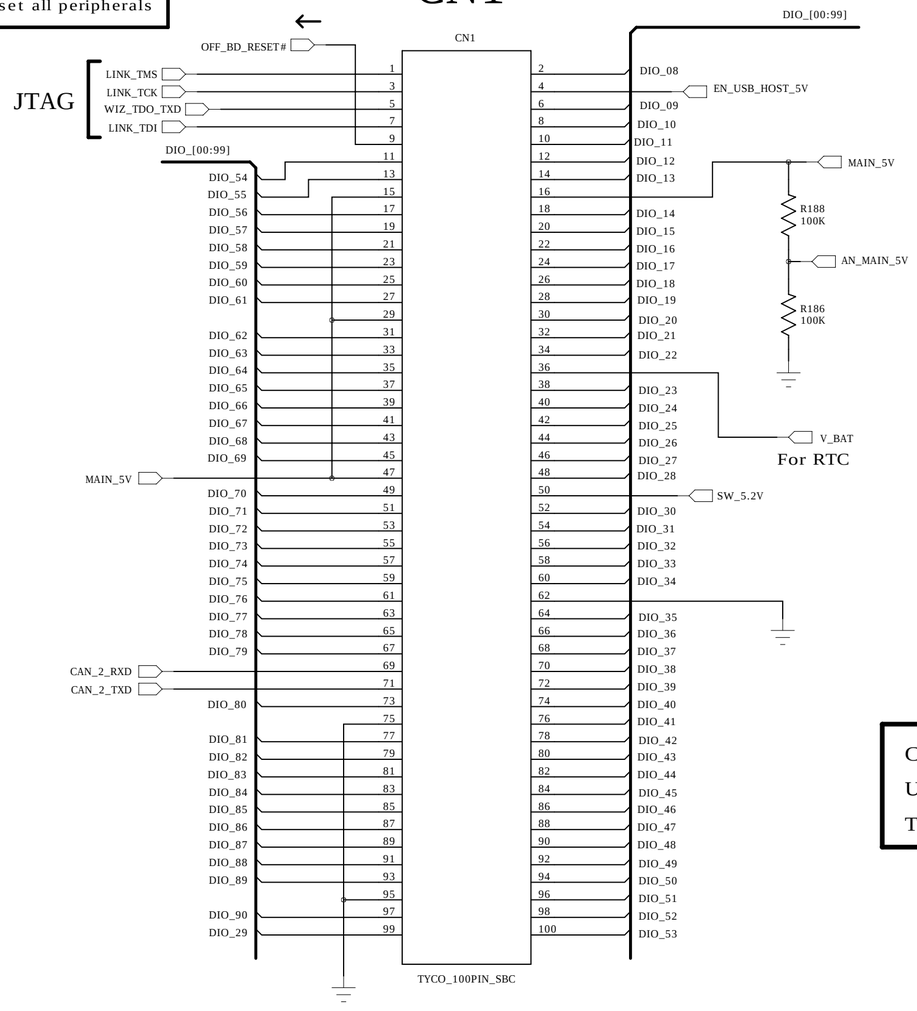
MAIN_5V pins supply power to the module
Apply 4.8V to 5.3V to these pins

Current drain is approximately 800 mA?

All pins except diff pairs use 3.3V levels

OFF_BD_RESET# is an Output used to reset all peripherals

CN1



3.3V rail can supply up to 500 mA to base board

USB = 90 ohm

See Sheet 5 for Diff Pair lengths

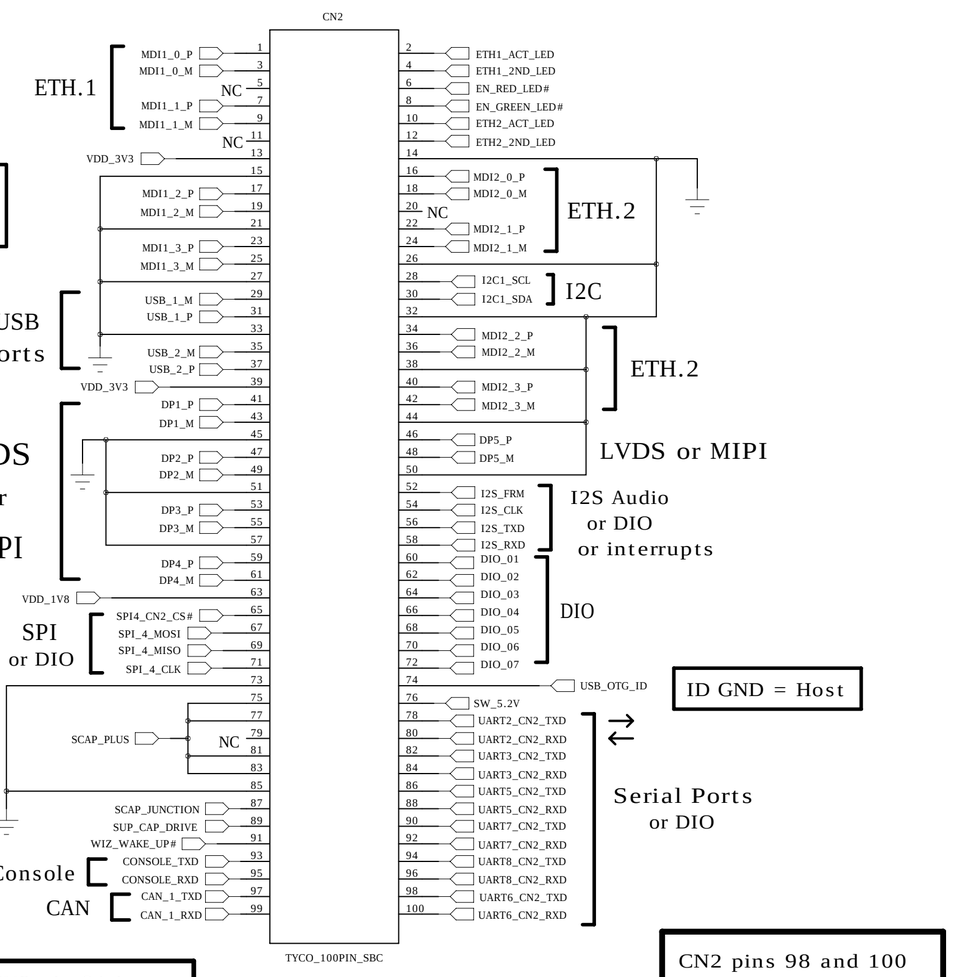
Diff Pairs = 100 ohm

CN1 pin 50 and CN2 pin 76 are
USB_OTG_5V on TS-4100
TS-4300 instead uses SW_5.2V

CN1 pin 67 is TXEN for RS-485 using UART2 on CN2 - maybe MAX10 can use UART7 HS2 ?

CN1 pin 17 (DIO_56) is "No CHRG" jumper on TS-8551
CN1 pin 19 (DIO_57) is "U Boot" jumper on TS-8551
CN1 pin 98 (DIO_52) is "SD Boot" jumper on TS-8551

CN2



ID GND = Host

CN2 pin 91 is Wiz uC Wake-up = active low

UARTs 3, 5, 7, 8
TXD is always an output using Level Shifters (U12-14)
RXD always an input (to U29) when using as DIO, RXD pins can be interrupts

CN2 pins 98 and 100 UART6 shared with BT
If using BT
Both pins can be DIO or UART7 HS lines or interrupts to CPU

UART2 is direct from CPU (at 3V levels)

UART6 TXD and RXD are directly from MAX10
If BT is used, iMX93 UART6 is not available

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Change Log for TS-4300 SOM:

Created Rev P1 December 2023

Started with TS-9370 Rev.P1

Changed board size to be TS-Socket

Used TS-4100 and TS-4900 as references

Modified Super Cap circuit using Booster

Added U37 for Board ID

Rev P1 BoM Population Updates ECO-DUAL-00 January 2023

Created two Configuations, TS-4300-DMWXI and TS-4300-DXWXI

K1, WiFi Module populated on all configuations

TS-4300-DMWXI populated with 1GB RAM and 16GB eMMC

TS-4300-DXWXI populated with 2GB RAM and 32GB eMMC

R42 TSPN attribute updated to 60-0036-5

R186-194 TSPN attribute updated to 60-0037-7

RN3-5, RN7 TSPN attribute updated to 60-0038-3

U9 TSPN attribute updated to Sample_PIMX9352CVVXMAB

R77 DNP on Option 2 for Strapping

Added temporary strapping table on Sheet 10 and Title Page

Change Log for TS-4300 P2 - Sept 2024

Started with TS-4300 Rev.P1

- Changed paradigm for programming CPU/FPGA
  - On P1, we could only program Wizard via USB, then Wizard programmed CPU/FPGA via JTAG
- Changed USB C to be same as TS-9370_P3 except 25V Ctl line = Wiz.only
  - This is same as TS-Proto_iMX95_P1
- Changed Copper Straps (U38) from FPGA to Wizard - 9 bits same as TS-9370_P3
- Wizard pin-out changed - same as TS-9370_P3 (but added CPU_RESET on pin 28)
- Removed Tag-Connect (CN88)
- JTAG on CN1 includes entire chain: MAX10 --> iMX93 --> Wizard
- Changed SD card to Push-Push
- CPU ADC pins now match TS-9370/90
- Changed Wizard LED (LED3) color to Yellow
- Wiz_Reset IC (U86) removed
- I2C1 used for CN2, I2C4 used for Wizard = new standard (TS-9370/90 will adopt this paradigm)
- Changed Option Res. straps (R73-R81) to be same as TS-9370/90

TS-4300 P2 BoM Clean-Up - ECO-DUAL-00103-B

- RN29 TSPN updated to be 60-0032-0
- RN20 RN23-25 TSPN updated to be 60-0038-3
- R41 TSPN updated to be 60-0036-5
- U77 TSPN for option 1 configuration updated to be Alliance 1GB LPDDR4X, 37-0016-4
- U77 TSPN for option 2 configuration updated to be Alliance 2GB LPDDR4X, 37-0018-6
- U9 TSPN updated to be 33-0029-6

Change Log for TS-4300 SOM:

Schematic Updates Rev P2 May 2025

Updated U9 Part to pull in Decal Updates

Decal B - text on NVCC_AON changed to show 1.8V or 3.3V

Created Rev A - March, 2025

Started with TS-4300 Rev.P2

Changed:

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