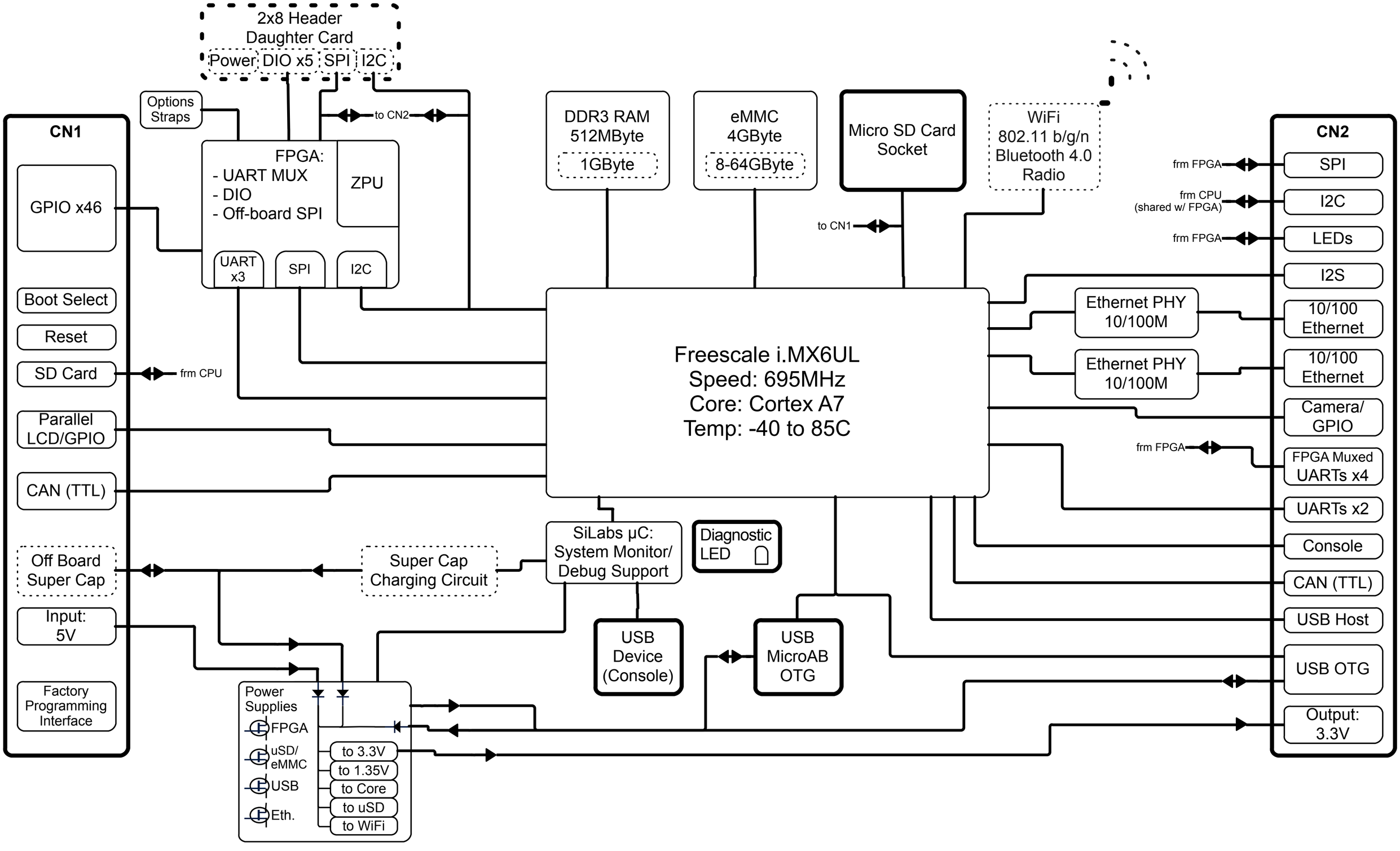
TS-4100 Rev B



Web Schematic: Some proprietary information has been withheld.

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Standard Options

Option 1	TS-4100-SMN1I	NXP i.MX6UL 695MHz ARM Cortex A7 512MB DDR3 RAM and 4GB eMMC Flash, (-40 to 85C)
	TS-4100-SMN2I	NXP i.MX6UL 695MHz ARM Cortex A7 512MB DDR3 RAM and 4GB eMMC Flash, Stand Alone w/ Daughter Card support (-40 to 85C)
Option 2	TS-4100-SMW5I	NXP i.MX6UL 695MHz ARM Cortex A7 512B DDR3 RAM and 4GB eMMC Flash, TS-SILO, WiFi/Bluetooth w/Chip antenna, (-40 to 85C)
Option 3	TS-4100-SRW9I	NXP i.MX6UL 695MHz ARM Cortex A7 1GB DDR3 RAM and 4GB eMMC Flash, TS-SILO, WiFi/Bluetooth w/Chip antenna, (-40 to 85C)
	TS-4100-SRW8I	NXP i.MX6UL 695MHz ARM Cortex A7 1GB DDR3 RAM and 4GB eMMC Flash, TS-SILO, WiFi/Bluetooth w/Chip antenna, Stand Alone w/ Daughter Card support (-40 to 85C)

Optional Components/Features Summary

All Parts are Industrial Temp

WiFi/Bluetooth Option

w/ Chip Antenna

U.FL available on request

Included only on xxx5x, xxx8x, xxx9x Standard Option

ADD: K2 (chip antenna)
(alternate: U.FL antenna connector)

1 GByte RAM Option

Included only on xRx8x, xRx9x Standard Option

REMOVE: U23 4Gbit Die

ADD: U23 8Gbit Die

TS-SILO Option

Included only on xxx5x, xxx8x, xxx9x Standard Option

ADD: U16, U9,
REMOVE: R37

Daughter Card Option

Makes an SBC configuration

w/ header for expansion

Included only on xxx2x, xxx8x, Standard Option

ADD: HD1

Web Schematic: Some proprietary information has been withheld.

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Rev.A to Rev B Changes

SiLab Power_FAIL needs series resistor to CPU (when no 3.3V prsent)

Change FPGA 3.3V to be always ON

Add 2 resistor straps for total of 4

AN_SCAP_1 should be going to CN2_87 (error on Rev.A)

ETH_PHY_IRQ should not be connected on either PHY chip

PHY should use FPGA DIO for Reset = "soft reset"

Make it easy to have SuperCaps on the base board

Add series resistor in 6UL_RESET#

Remove U19 (FPGA reset IC)

Must be able to switch power to eMMC

Add ID pin to identify Rev.B - PD on SPI MOSI

Add OFF_BD_RESET# 47K PD res

Remove U18 - PHY now using soft reset

Isolate CPU 3.3V current using R22

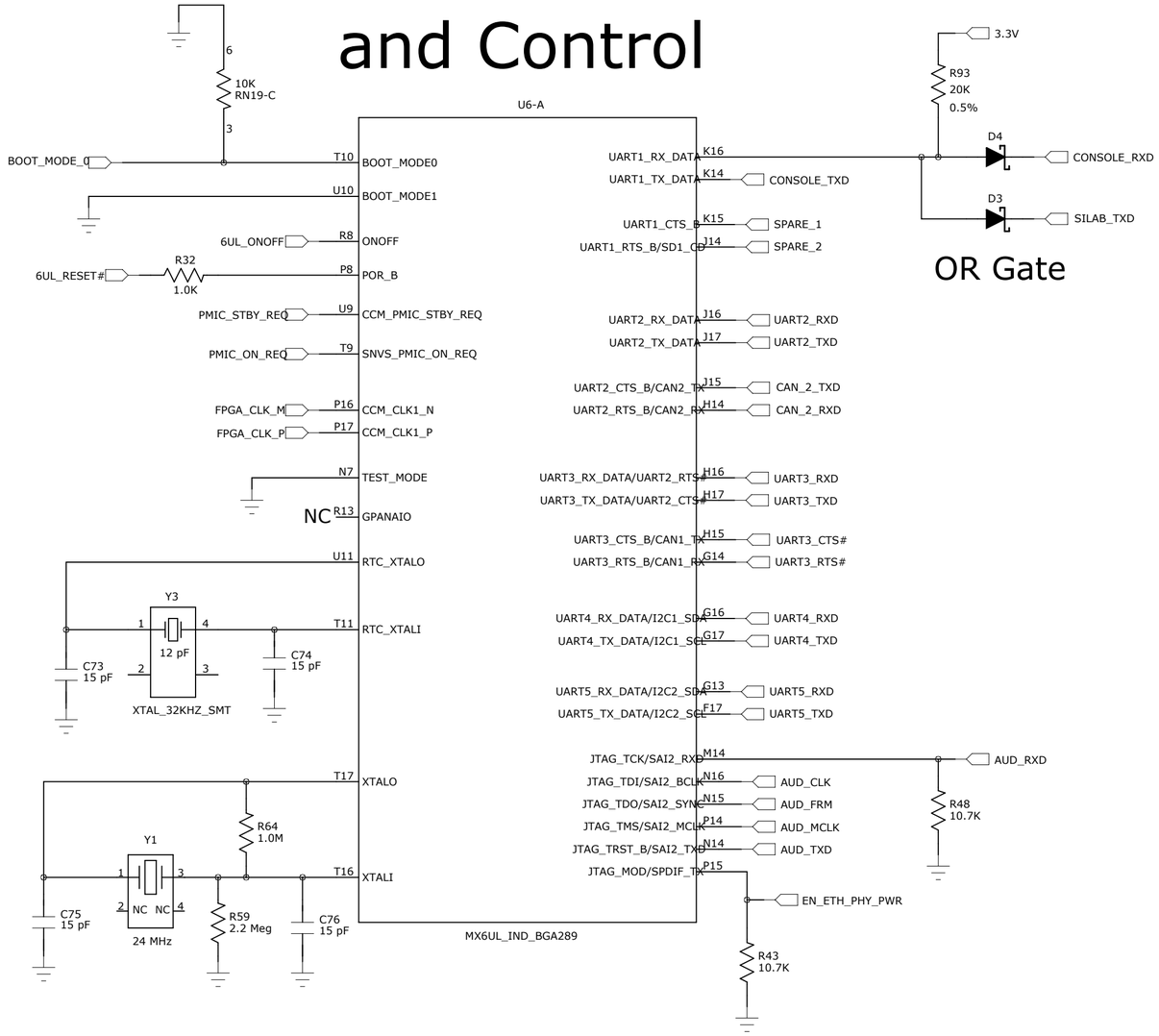
Change CAM_VCC rail to isolated 3.3V

Change C47 to 470 pF 0603 ?

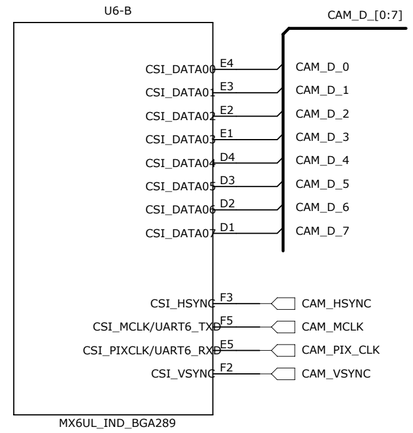
Move "No CHRG" jumper to CPU or FPGA - Change CN1-17 to SPARE_1

Remove K1 and R33 (no more 24 MHz Osc) - use Xtal instead

6UL UART and Control



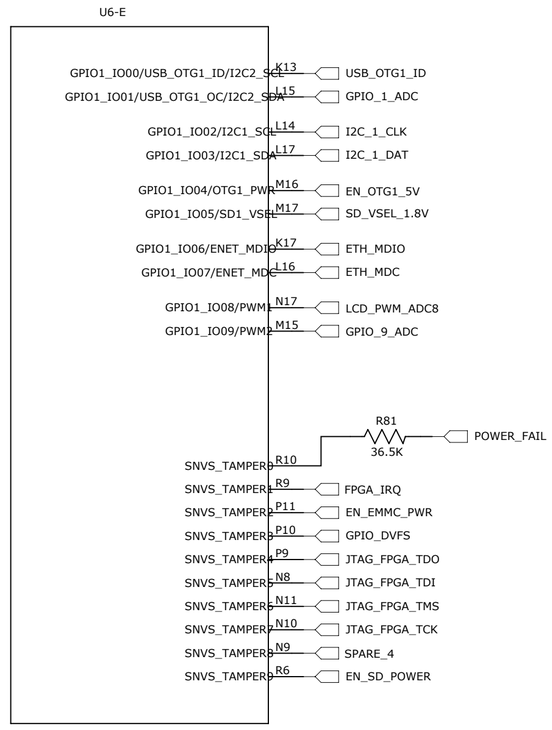
6UL Camera



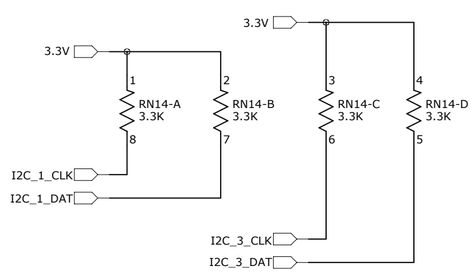
32 KHz

24 MHz Osc.

6UL DIO



I2C PU Res.



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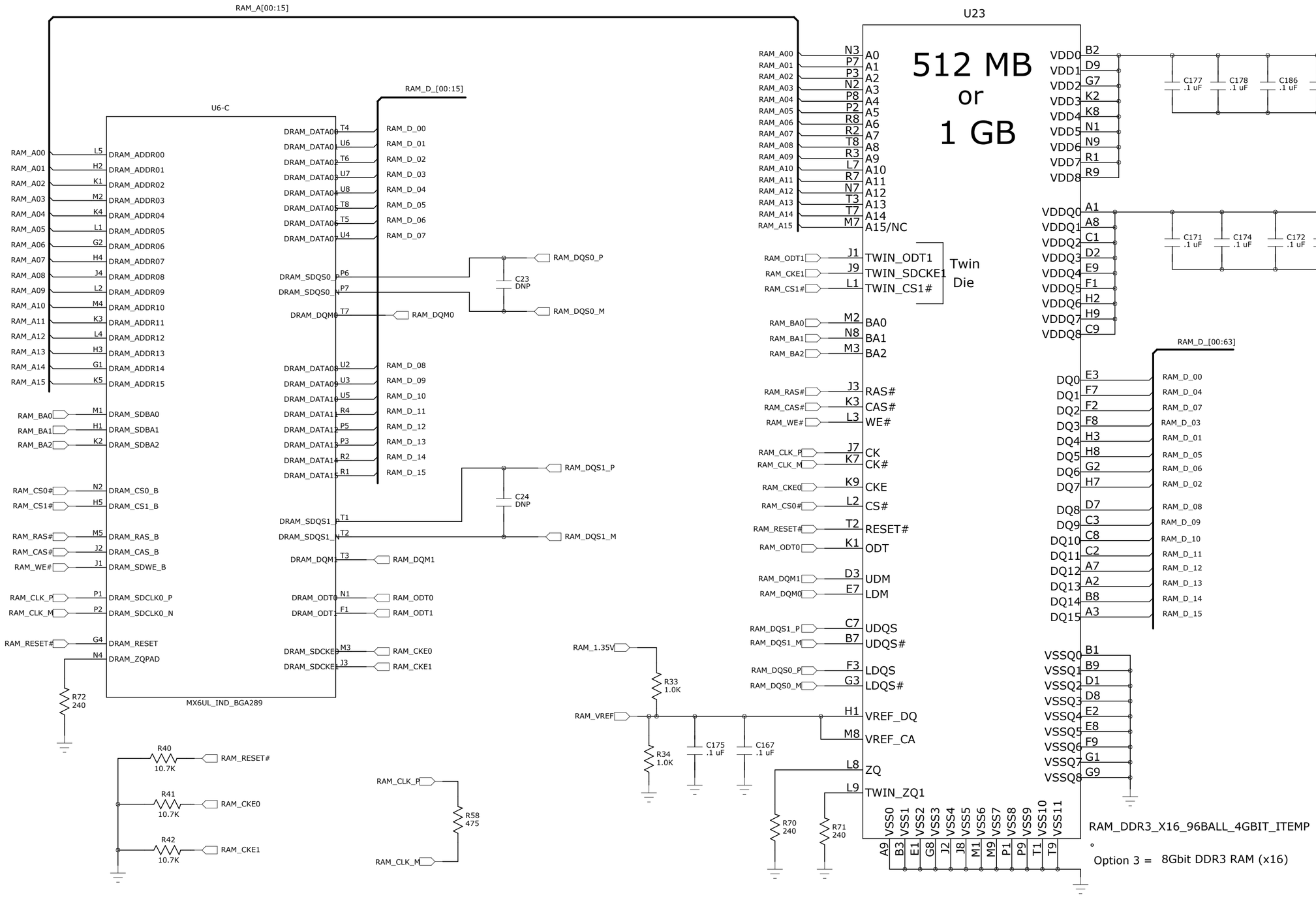
6UL RAM Interface

DDR3 RAM



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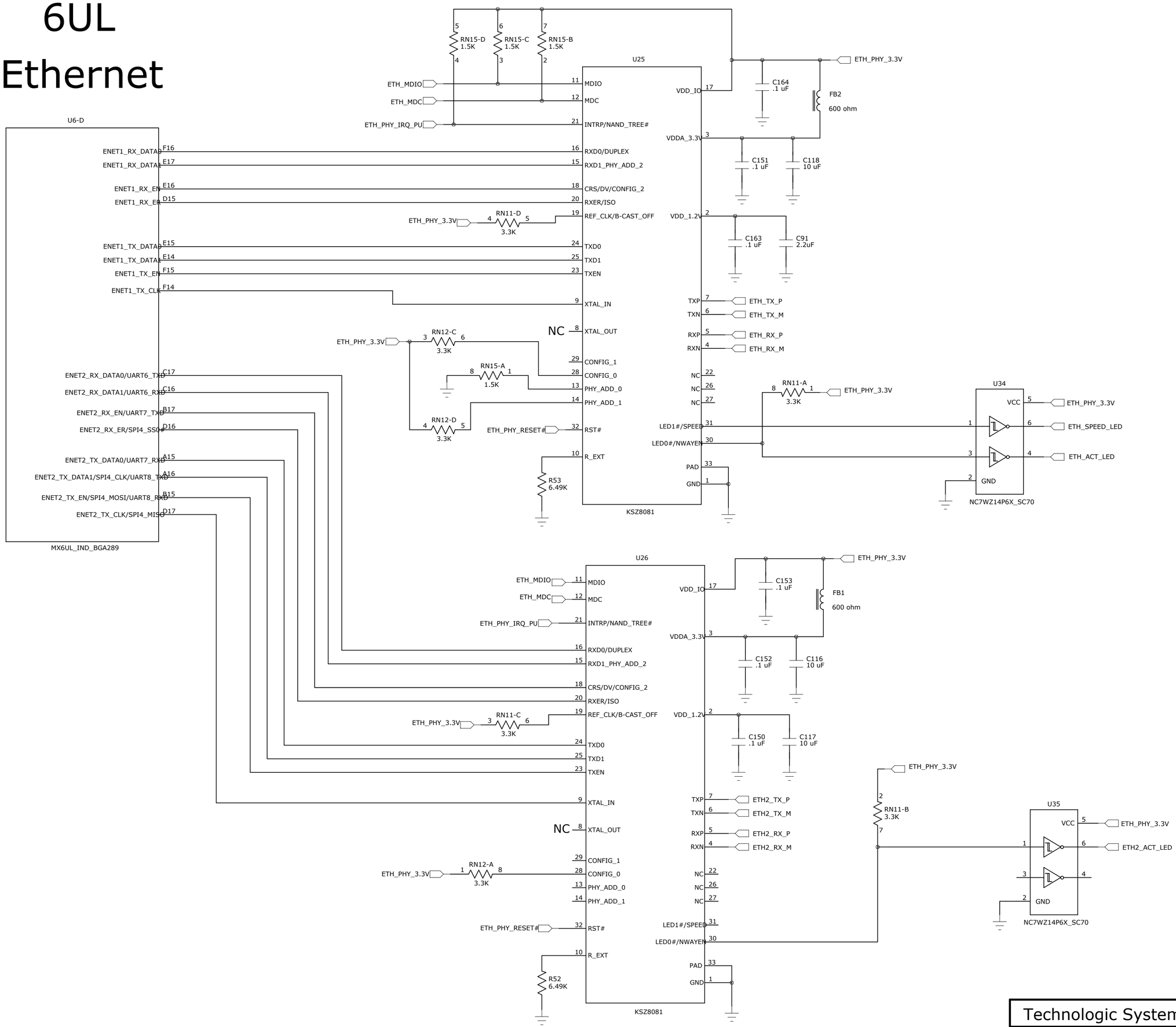
6UL Ethernet



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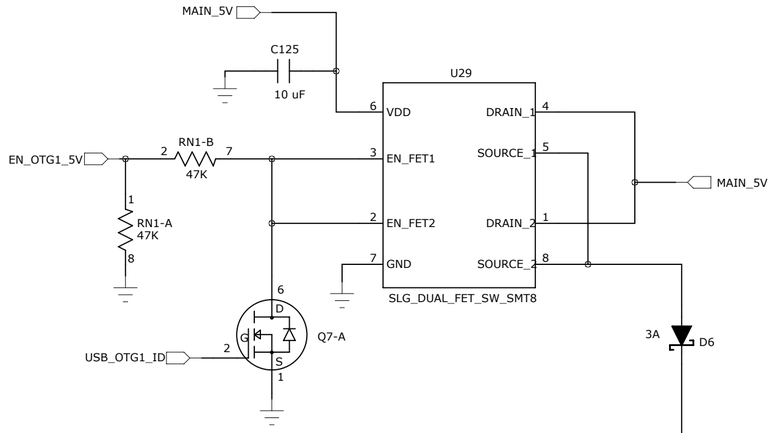
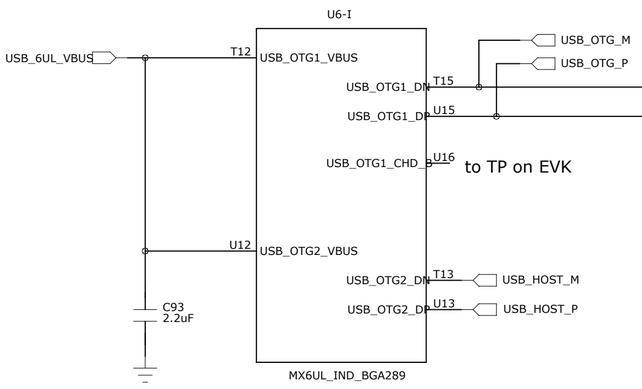
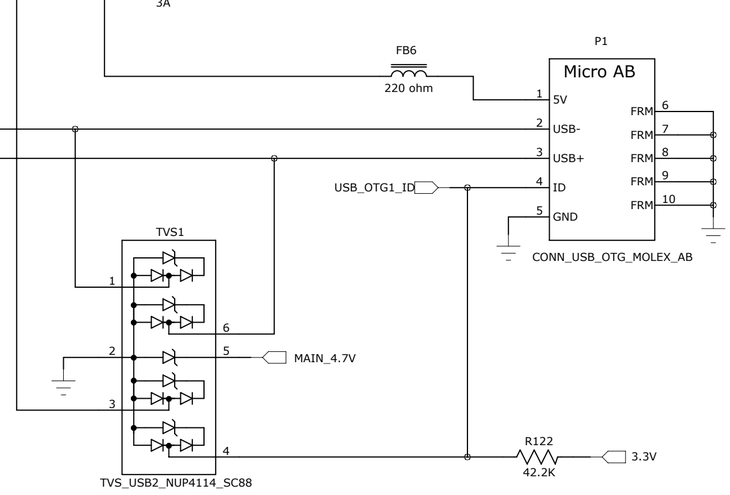
USB 5V Switch



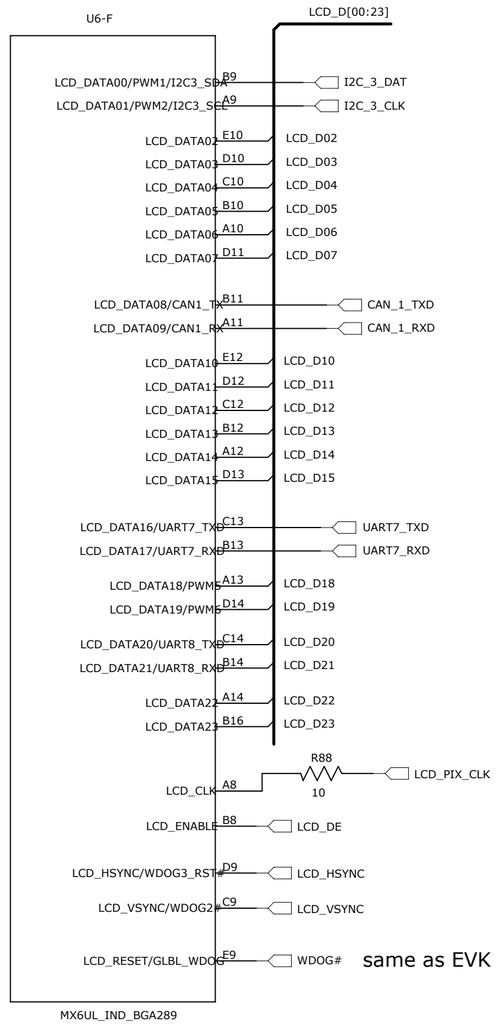
6UL USB Ports



USB OTG Micro AB



6UL LCD



Host USB 5V comes from 5V switch

Turns on when 3.3V present

directly drives Host USB port

and also drives USB_OTG2_VBUS ball

OTG1_VBUS comes up from BB.

It is gated off until 3.3V present

It also goes thru a diode

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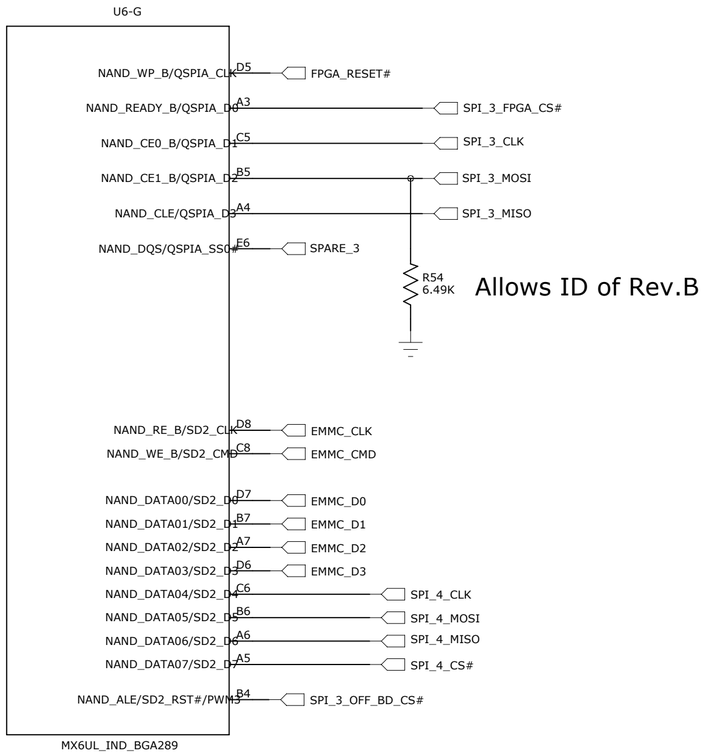
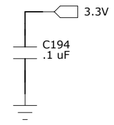
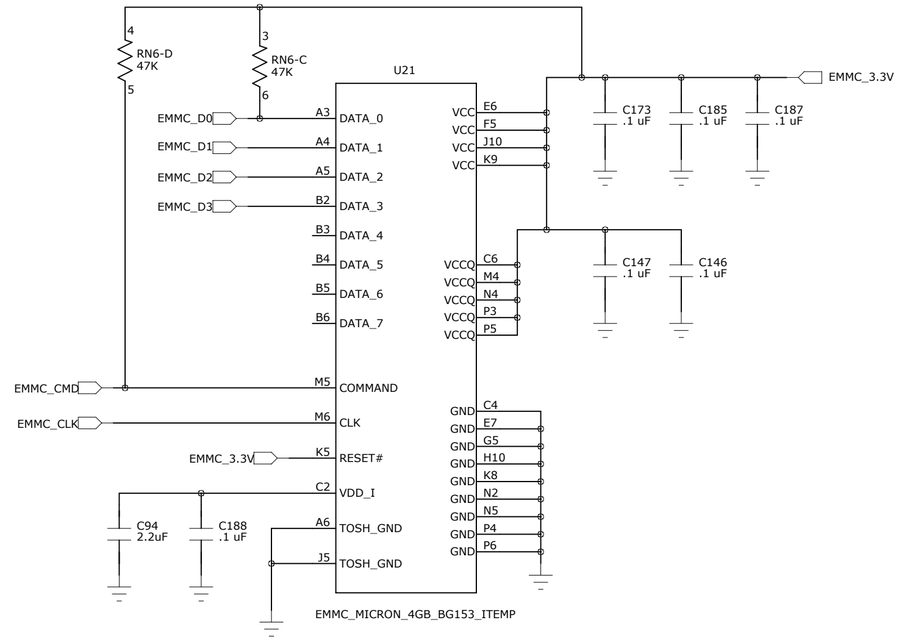
6UL Flash



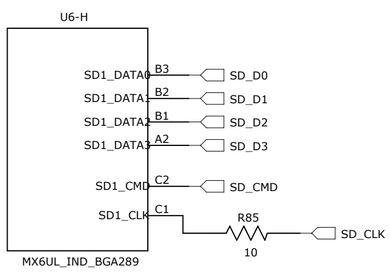


eMMC 4GB

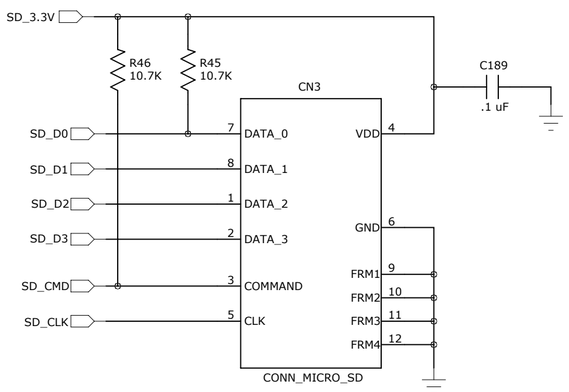
(optional: up to 64GB)



6UL SDIO



Micro SD Card Socket



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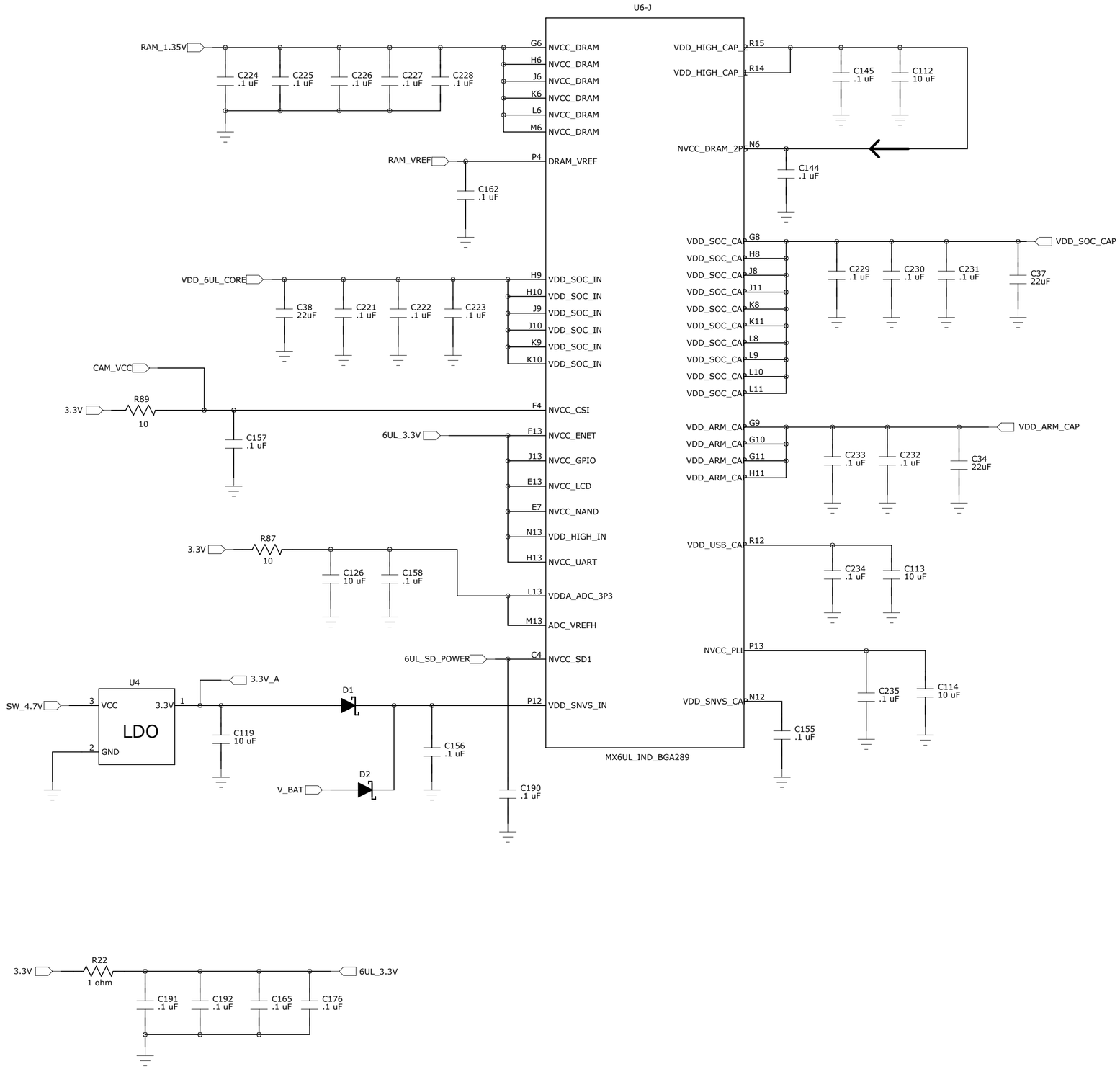
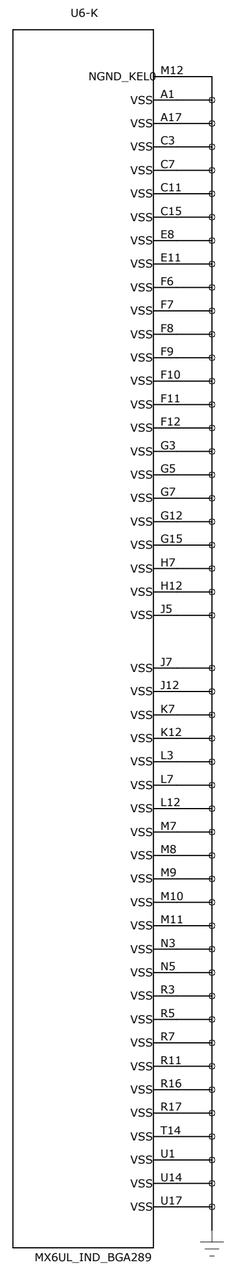
6UL Power



6UL GND



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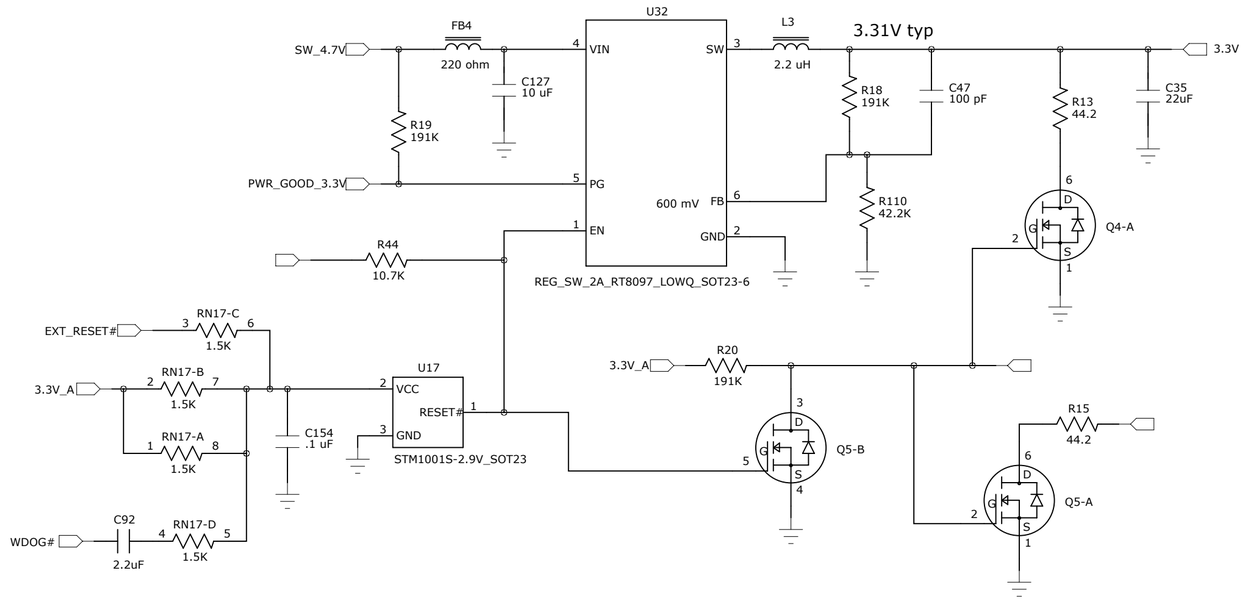
SD Card 1A Reg
1.8V or 3.2V

3.3V --> 6UL_SD_POWER

3.3V 2A Reg



CPU Core 1A Reg

SW_4.7V --> DCC_6UL_CORE

RAM 1.35V 1A Reg

SW_4.7V --> RAM_1.35V

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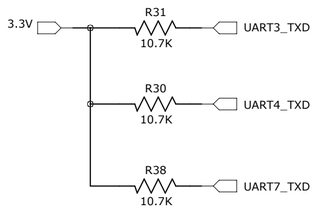
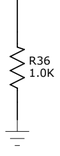
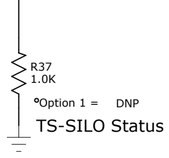
MACH XO2 FPGA

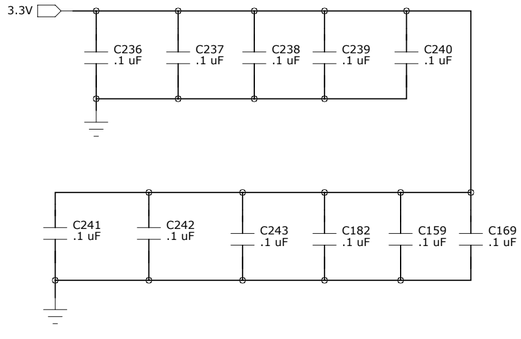
FPGA required for:

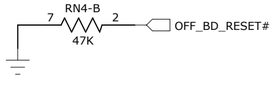
- Auto-485 for two UARTs
- Extra MAX3100 UARTs
- MUX for UARTs
- Additional I/O
- Off-board SPI











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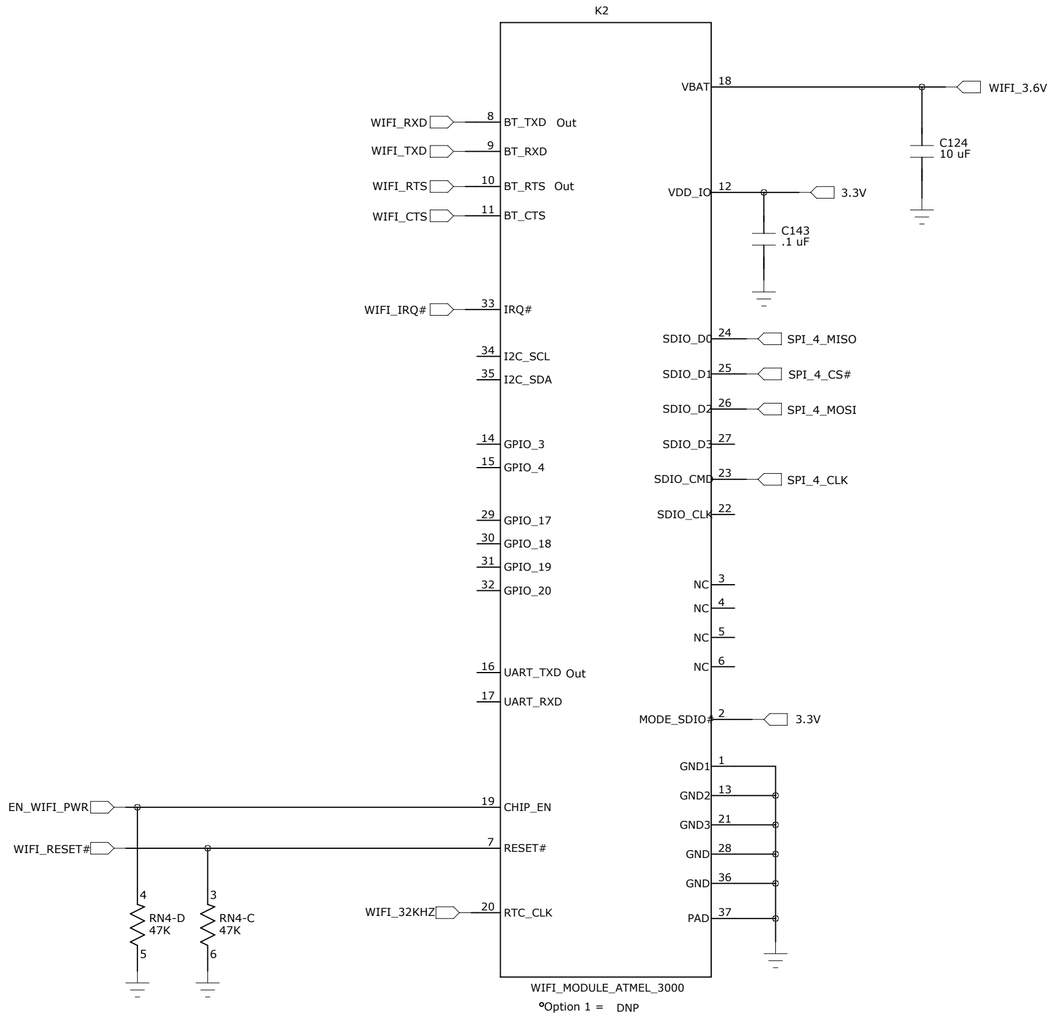
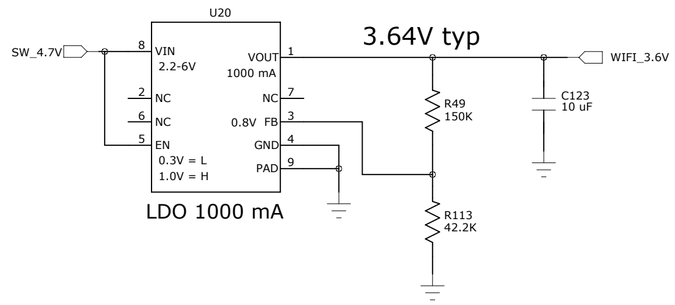
WiFi

WiFi / Blutooth Radio Module



WiFi 3.6V Regulator



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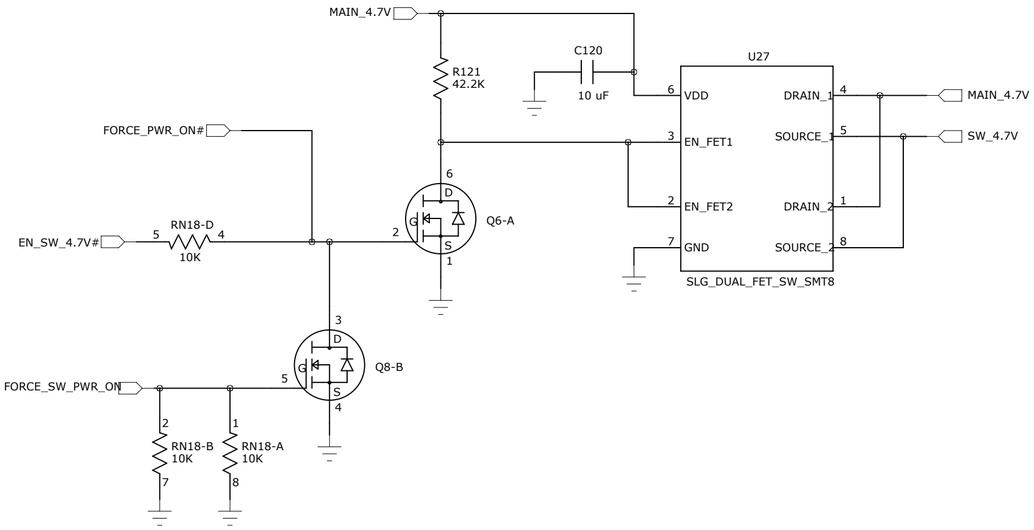
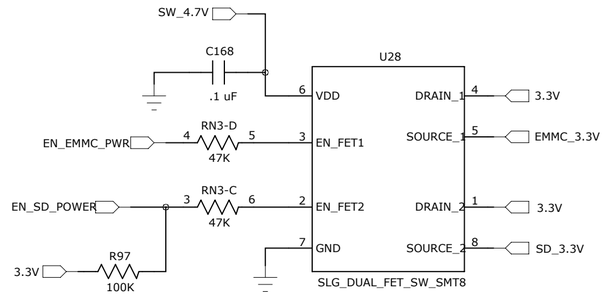
Main 4.7V Power Sw.

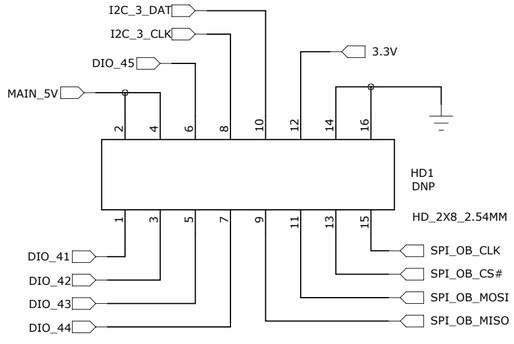


eMMC and SD Card Power Sw.

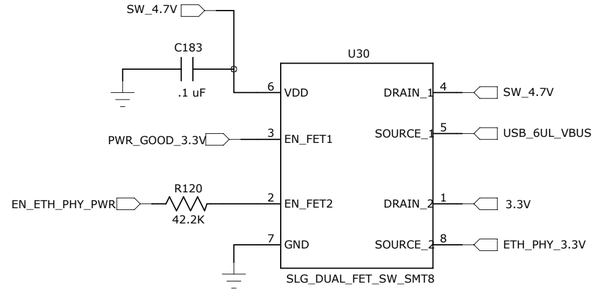


Daughter Card Interface

16 pin Header



USB VBus and Eth Power Sw.



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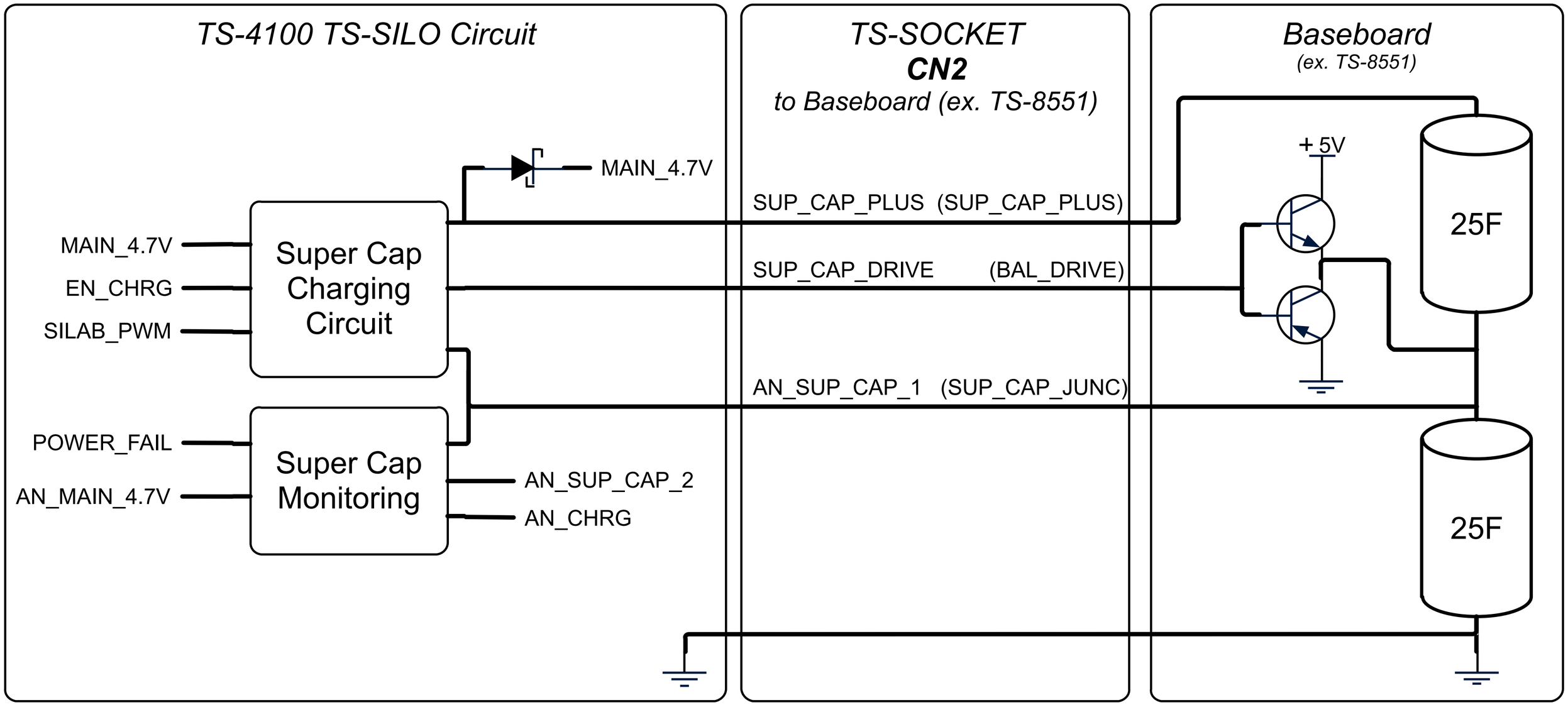
SuperCap Power Hold



2 watt load = 400 mA from 5V

After Power Fail, consumption can be lowered to less than 1 watt to give 20 seconds

Functions down to SuperCap = 3.5V

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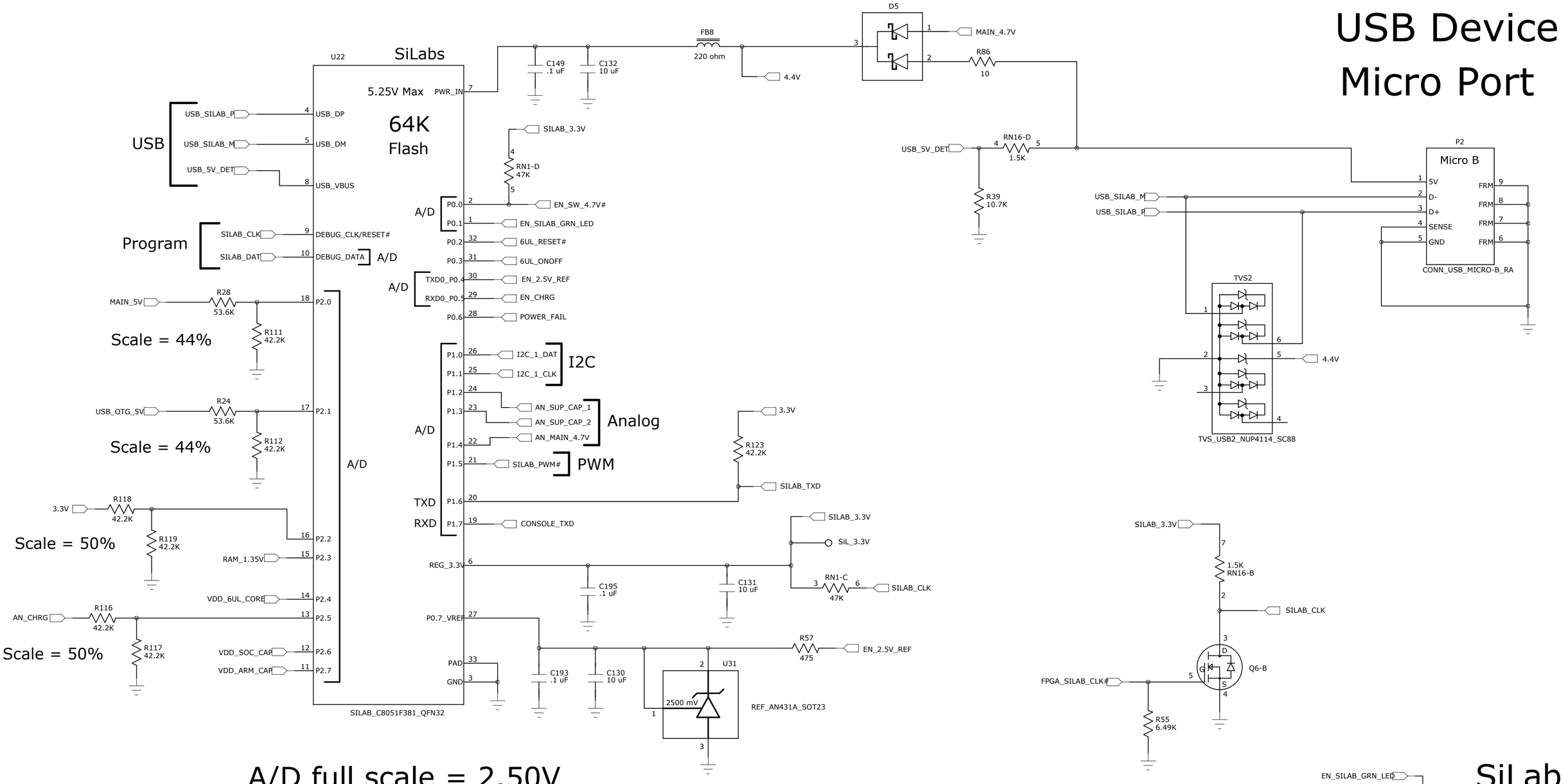
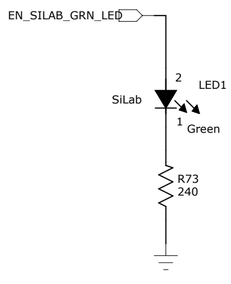
USB Device Port and SiLab uC

USB Device Micro Port



A/D full scale = 2.50V

SiLab LED



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Two 100-pin Off-board Connectors

⚠ All signals driving DIO on CN1 & CN2 must be powered by the 3.3V on CN2, or remain at 0V until the CN2 3.3V rail is > 3.0V

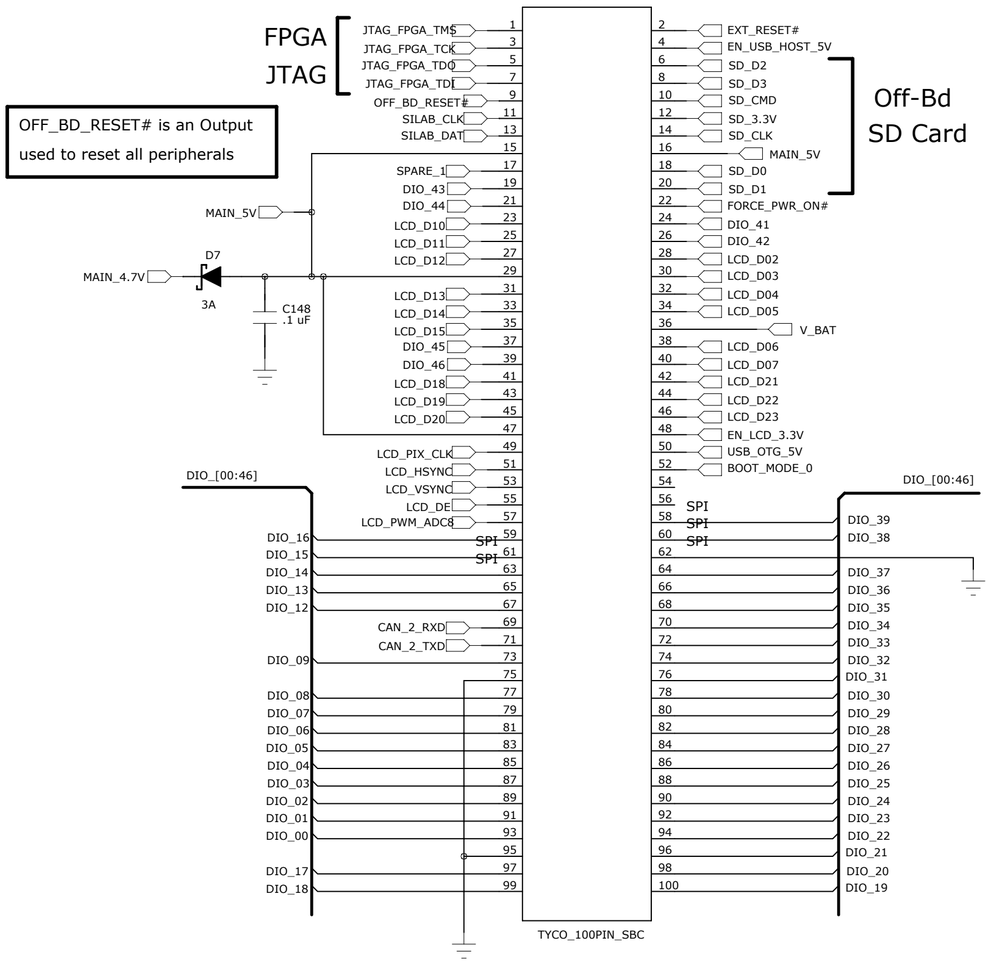
"POWER" pins supply all power to the module
Apply 4.7V to 5.3V to these pins

Current drain is approximately 300 mA

EXT_RESET# is an Input
used to reboot the CPU

Do not drive active high
(use open drain)

Left



OFF_BD_RESET# is an Output
used to reset all peripherals

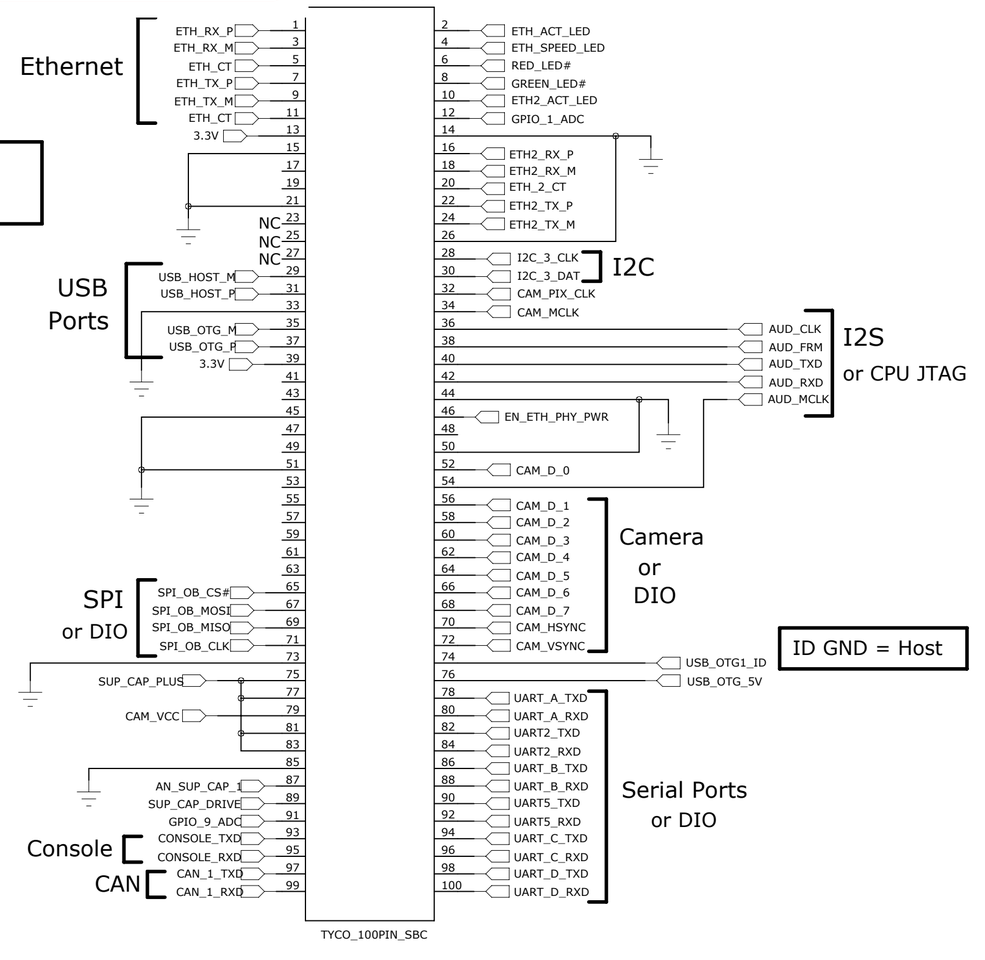
Off-Bd SD Card

SPI

Right

⚠ Pin 1 is the top left corner pin on the connector. All of the pins on the left are odd numbered. This may differ from the connector manufacture's datasheet.

3.3V rail can supply up
to 500 mA to base board



I2C

I2S or CPU JTAG

Camera or DIO

USB_OTG1_ID

ID GND = Host

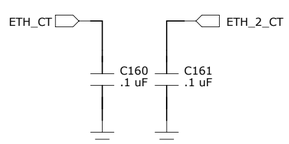
Serial Ports or DIO

Boot Strap

DIO_20	TS-4100 Boots from
1	eMMC Flash
0	SD Card

DIO_20 is latched prior to
OFF_BD_RESET# deasserted

⚠ Any I/O routed to a user accessible connector should have additional ESD protection placed on the carrier board.



Base board should connect CN2 pins 39 and 79 together if the CAM DIO should use 3.3V levels
If not connected, they will have 2.6V levels

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