March 2015

Changes from Rev.D to Rev.E

Added R28 = 45.3 ohm in series with RAM clock

This was required because 128 MB RAM version

would fail at -20 to -40 degrees

This was seen in about 40% of all 128MB boards

Problem was never reproduced in 64MB versions

Rev.E BOM changes

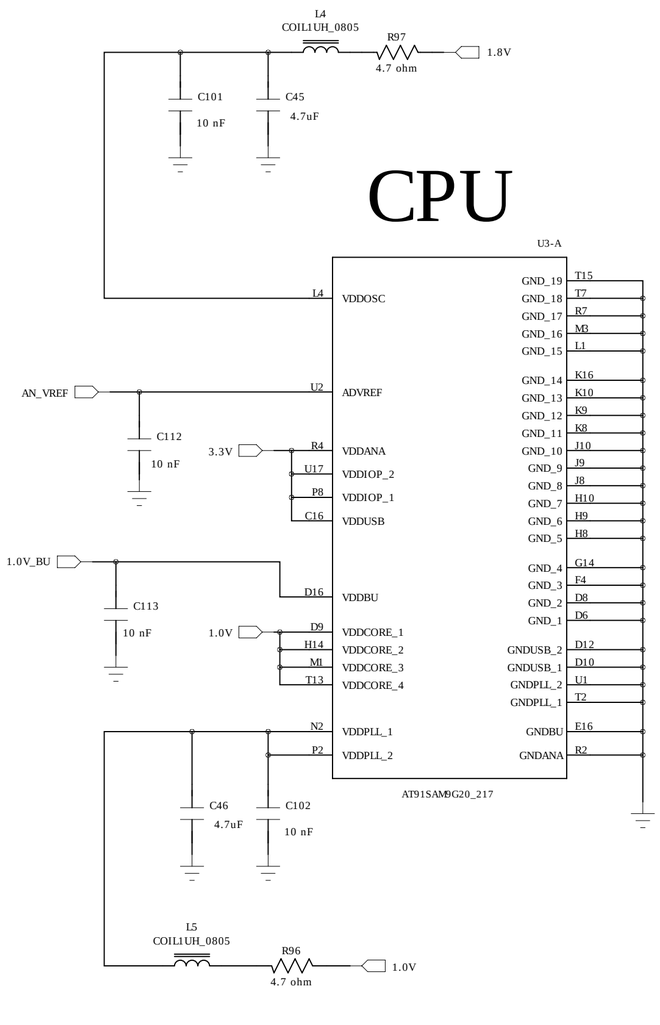
Only change to BOM is adding

R28 = 60-4770-4

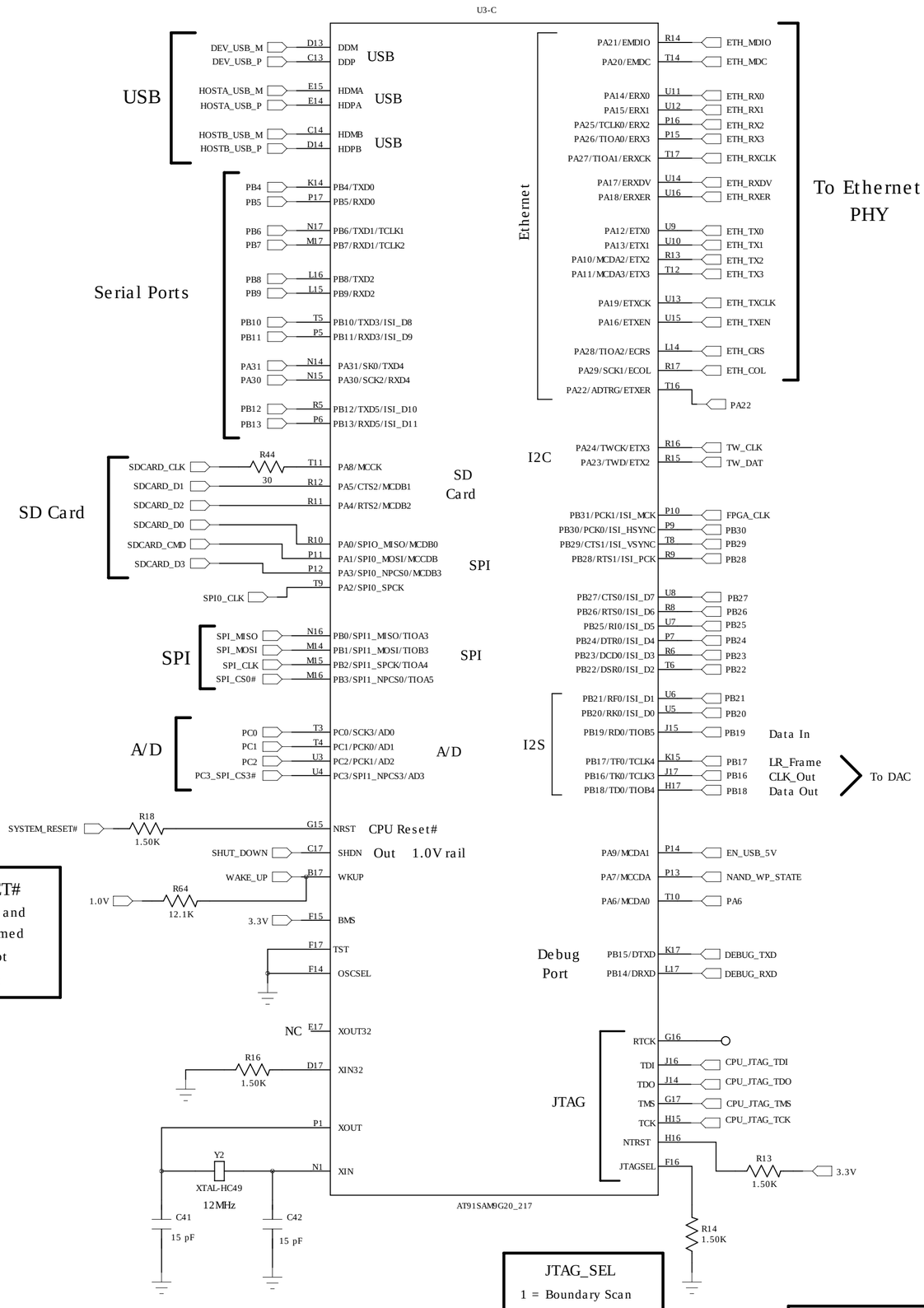
Technologic Systems		Date March 22, 2015
Title: TS-4200 CPU		
Rev: E	Designer	Sheet 1 of 8

TS-4200 Rev E

CPU



CPU



CPU_RESET#
is bi-directional and
can be programmed
to cause interupt
instead of reset

JTAG_SEL
1 = Boundary Scan
0 = CPU ICE mode

MT1 1 MT125
MT2 1 MT125

Technologic Systems	Date March 22, 2015	
Title: TS-4200 CPU		
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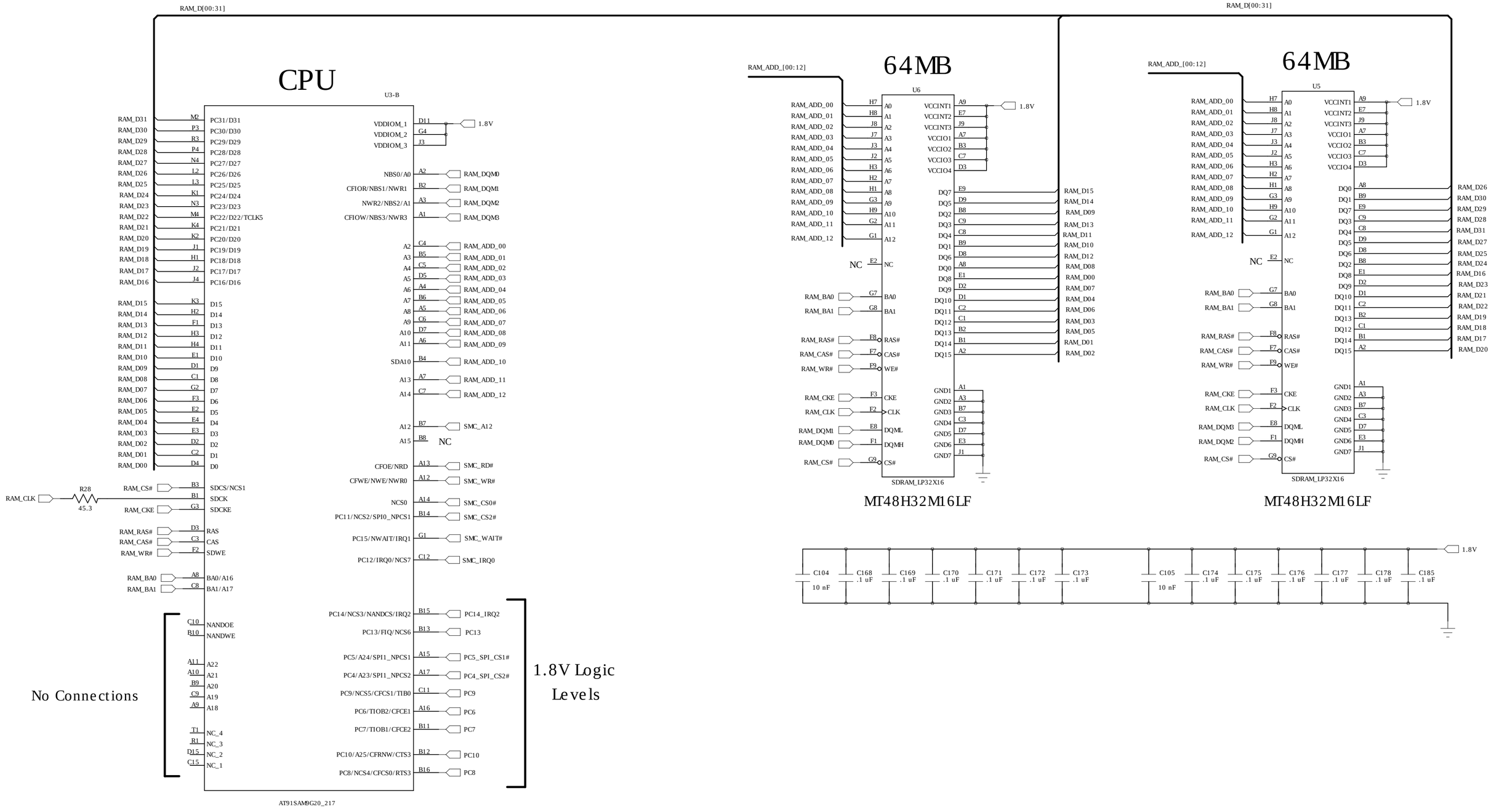
128 MB RAM



Technologic Systems		Date March 22, 2015
Title: TS-4200 RAM		
Rev: E	Designer RLM	Sheet 3 of 8

FPGA

A3P125 has:
3000 Tiles (about 1200 LUTs)
4 Kbytes total of Block RAM
97 I/O with 144 pin package
"true instant ON"
Input PLL clock = 1.5 MHz min

Warning: MUX_AD00 thru AD07 is used by NAND Flash

Devices connected to this bus must never drive it when BUS_RD# is deasserted
(must be off within 30 nS of deassertion)

Devices must pull the BUS_WAIT# line low if they need more than 150 nS strobe

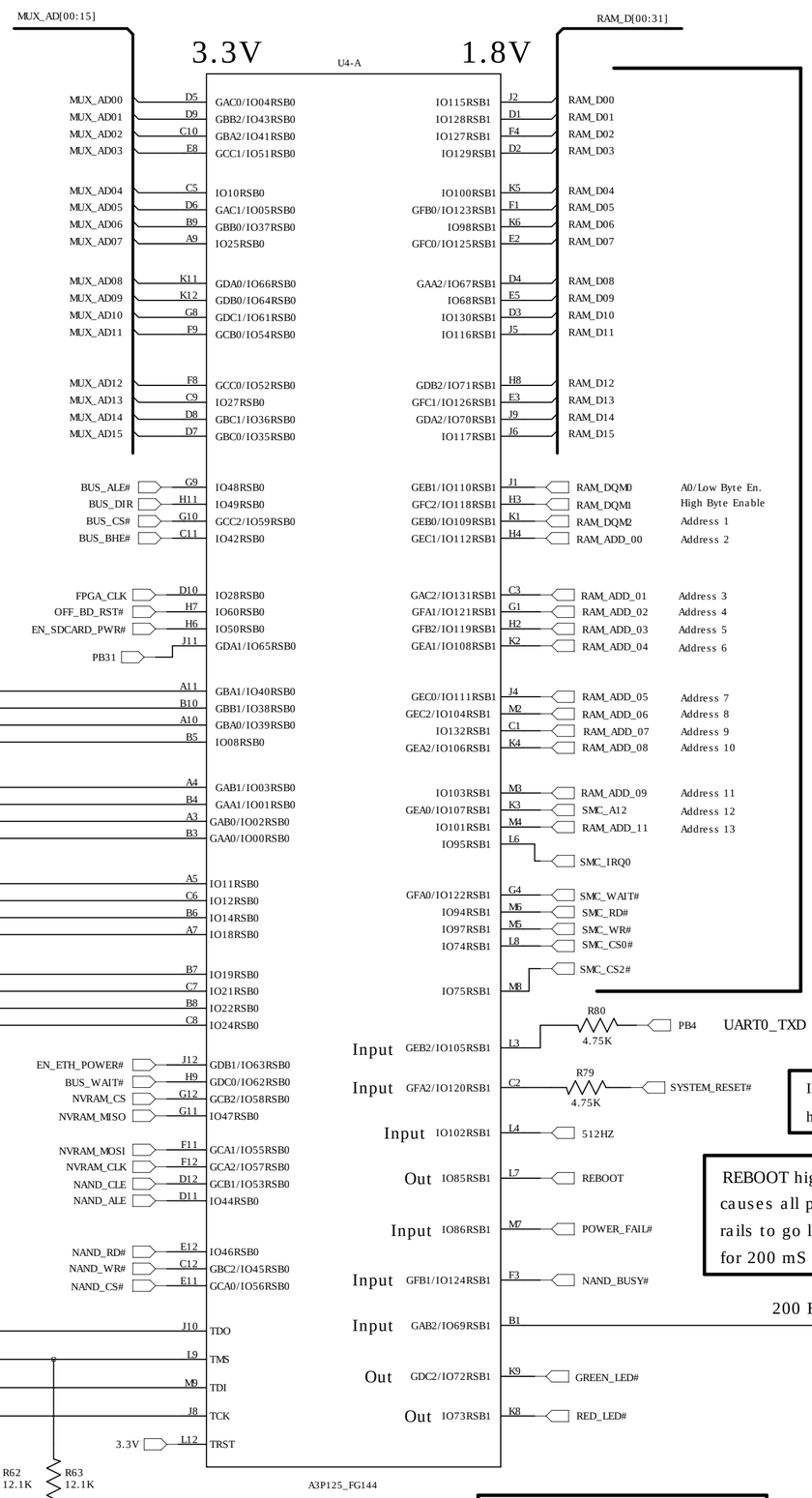
DIO_09 = Push_switch

When SYSTEM_RESET# deasserted,
Latch BUS_ALE# and BUS_RD#
into a register

Boot Straps

Mode 2	Boots from
1	NAND Flash
0	SD Card

BUS_ALE# = MODE1
BUS_RD# = MODE2



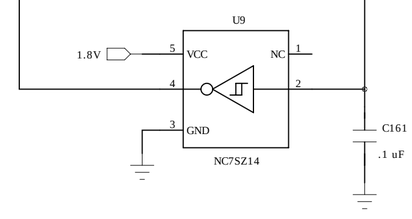
To CPU
Address/Data Bus

Inputs with 1.8V rail
have diode clamp to 1.8V

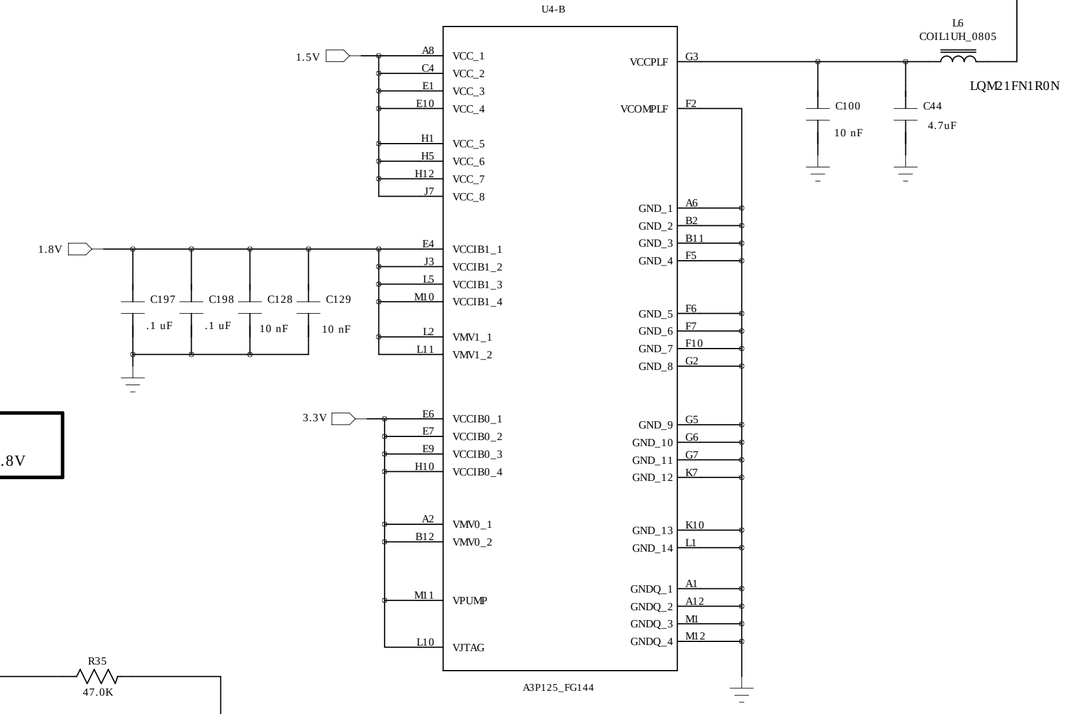
REBOOT high causes all power rails to go low for 200 mS

RED_LED# and GREEN_LED# must be Open Drain

200 Hz



FPGA



RMCF 1/16S 10 5% R
1.5V
R98
4.7 ohm
L6
COIL1UH_0805
LQM21FN1R0N
C100
10 nF
C44
4.7uF

Technologic Systems	Date March 22, 2015	
Title: TS-4200 FPGA		
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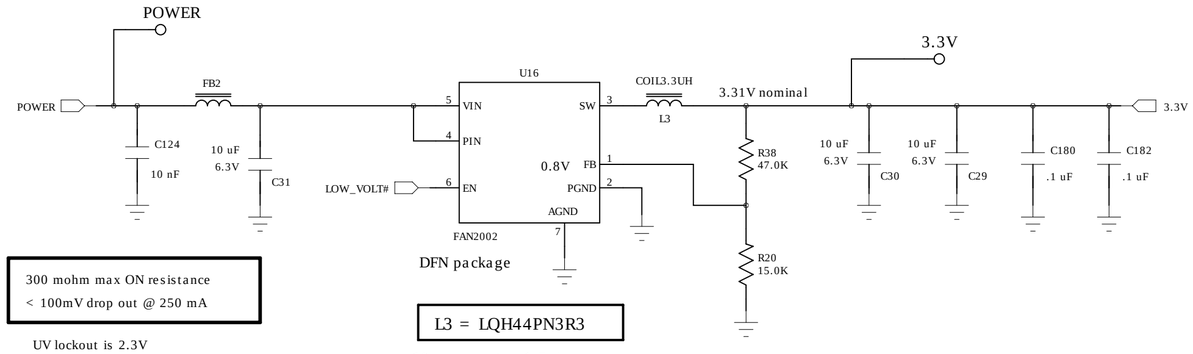
3.3V Supply

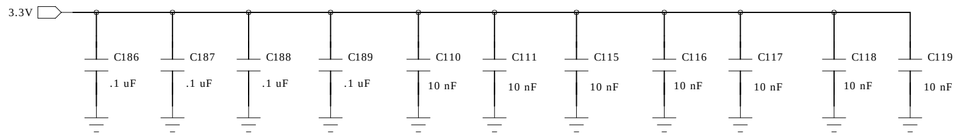


300 mohm max ON resistance
< 100mV drop out @ 250 mA

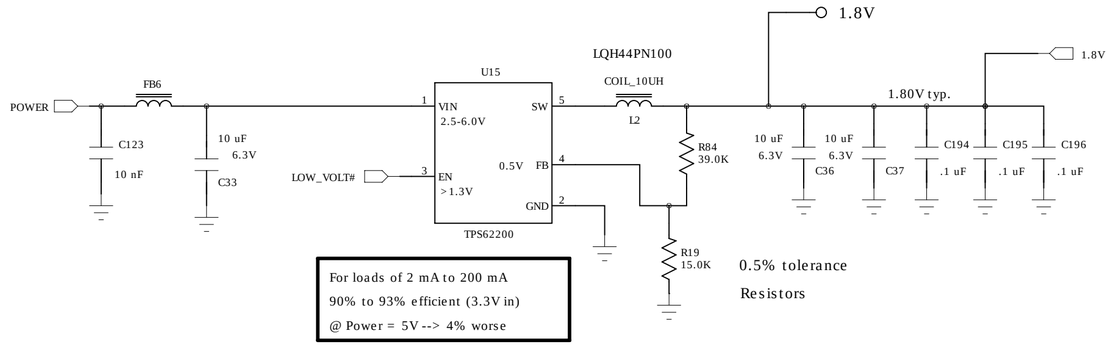
UV lockout is 2.3V

L3 = LQH44PN3R3

Max. current = 1.7 Amps



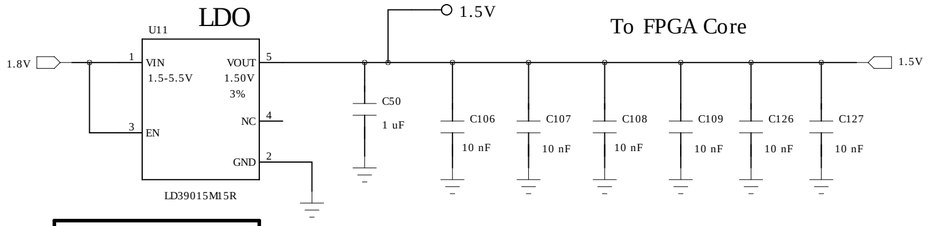
1.8V Supply



For loads of 2 mA to 200 mA
90% to 93% efficient (3.3V in)
@ Power = 5V --> 4% worse

0.5% tolerance
Resistors

1.5V Supply



150 mA max load
100mV drop out
stable with 1 uF ceramic
25 uS Turn-on

Power Sequence

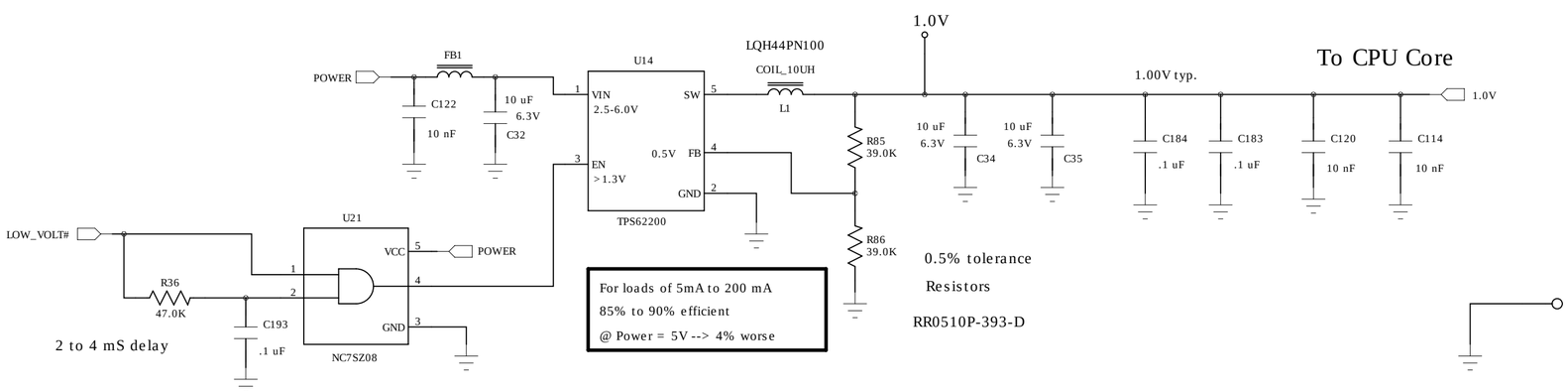
After power is first applied, or after a "Reboot"
All power rails are off for 200 mS then:

- the 3.3V and 1.8V are enabled
  these will reach 95% in about 800 uS
  (the 1.5V rail will ramp 25 uS delayed)

- Then 2-4 mS later, the 1.0V rail is enabled
  It also requires about 800 uS to ramp

CPU Reset# is asserted before 1.0V rail is enabled

1.0V Supply



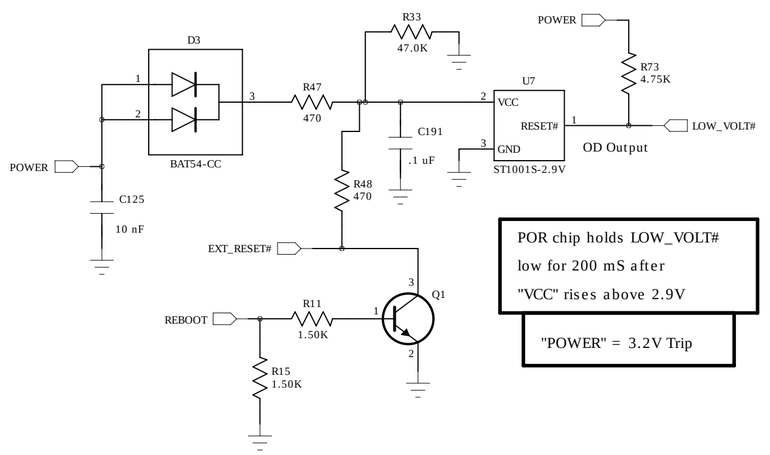
2 to 4 mS delay

For loads of 5mA to 200 mA
85% to 90% efficient
@ Power = 5V --> 4% worse

0.5% tolerance
Resistors

RR0510P-393-D

POR

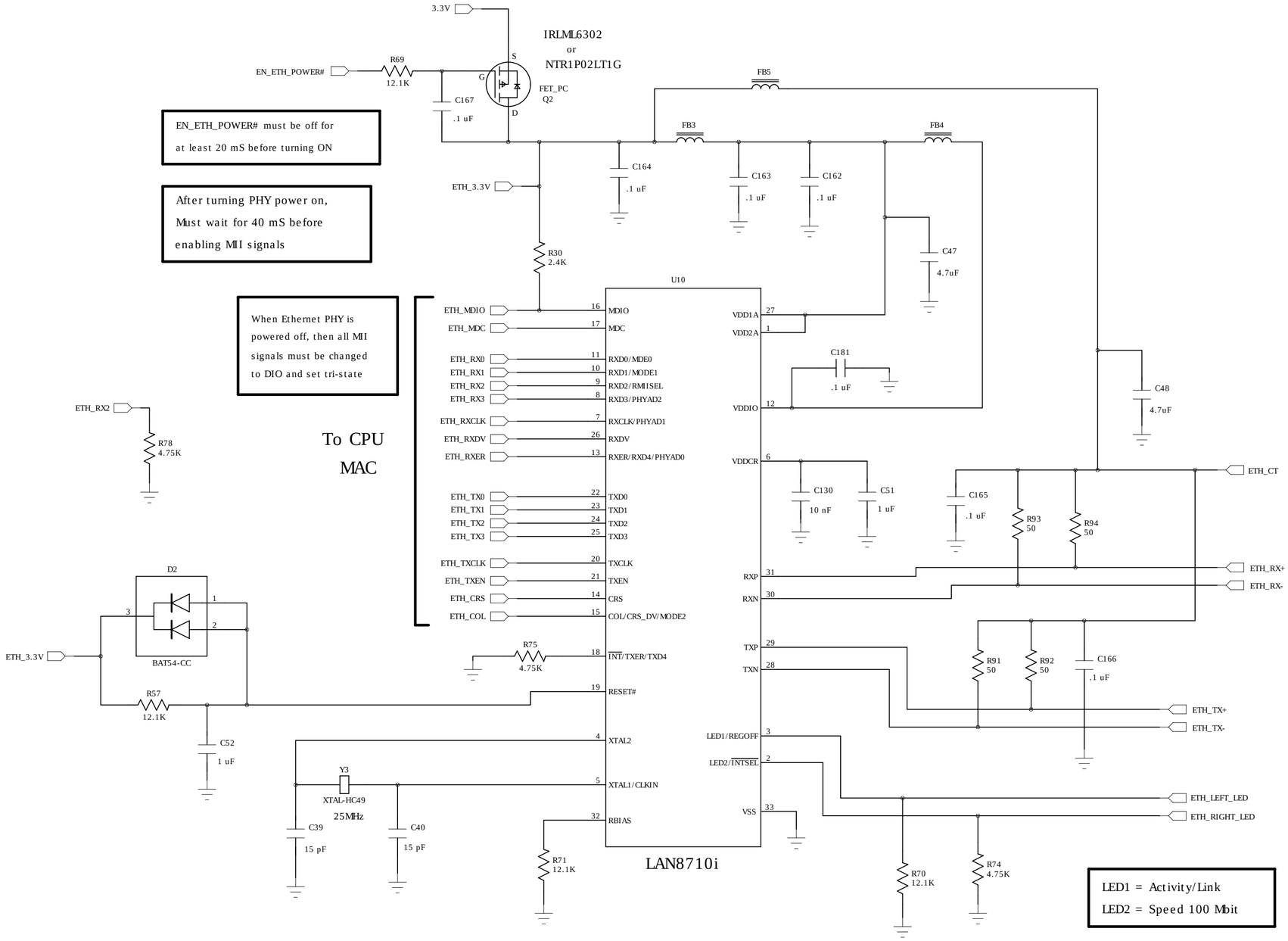


POR chip holds LOW_VOLT#
low for 200 mS after
"VCC" rises above 2.9V

"POWER" = 3.2V Trip

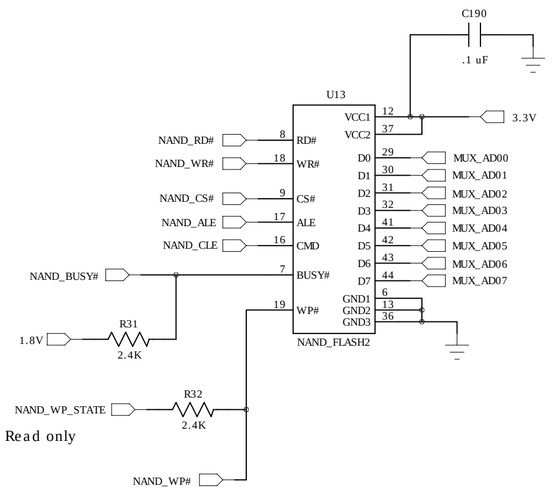
Technologic Systems	Date March 22, 2015	
Title: TS-4200 Power Supplies and POR		
Rev: E	Designer RLM	Sheet 5 of 8

10/100 Ethernet

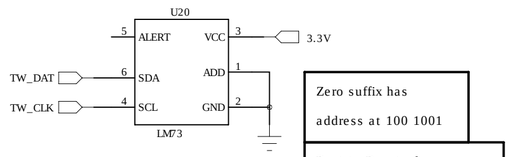


Technologic Systems		Date March 22, 2015
Title: TS-4200 Ethernet PHY		
Rev: E	Designer	Sheet 6 of 8

512 MB or 2 GB NAND Flash



Temp Sensor

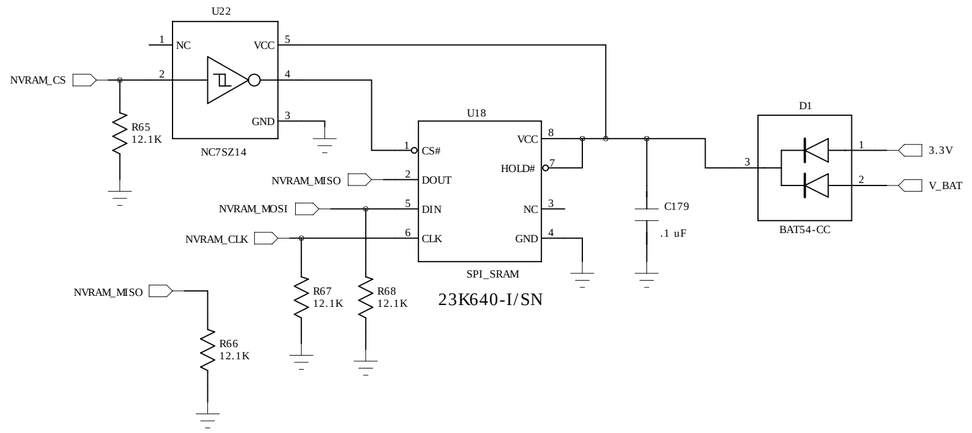


Zero suffix has address at 100 1001

Best to Reset after all power cycles

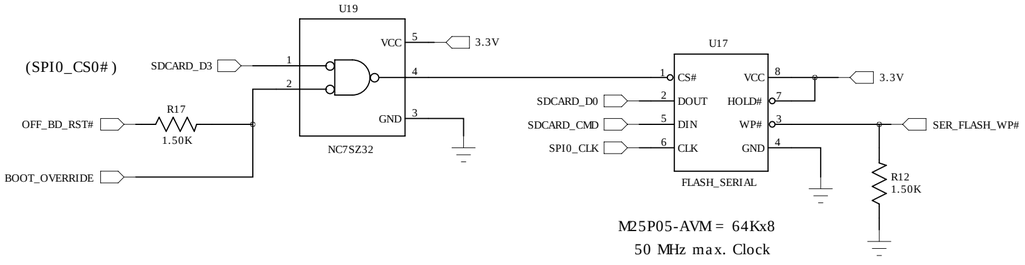
Set PD bit, Wait 50 mS
Then clear PD bit

8K Byte NVRAM

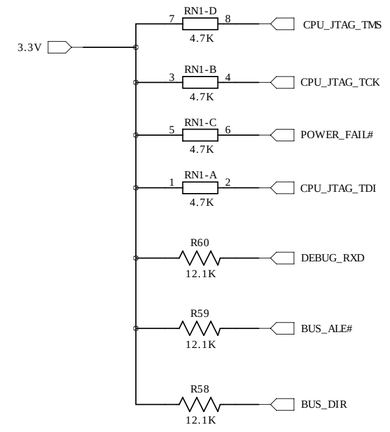


64KB Serial Boot Flash

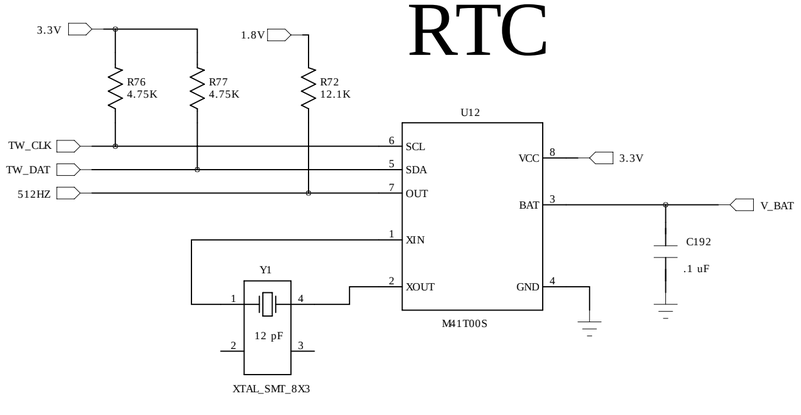
Boot using SPI0 Port



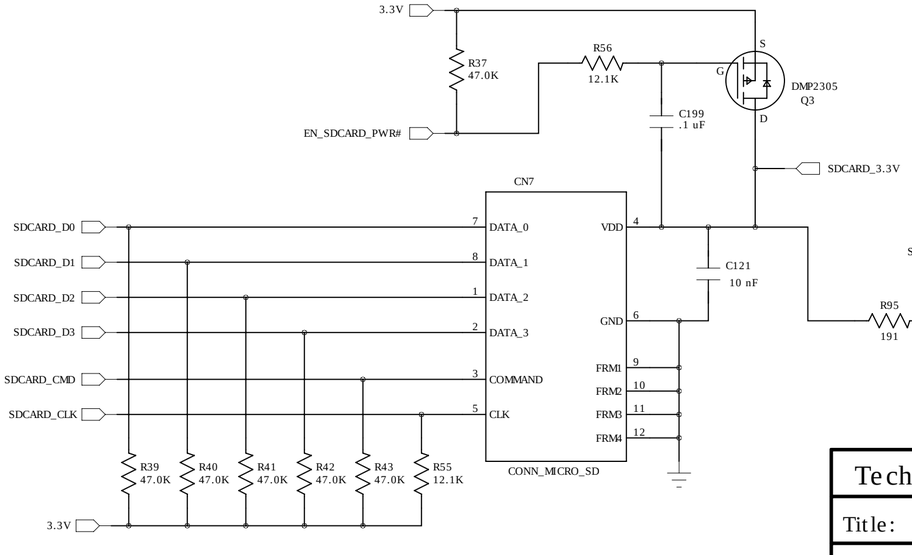
M25P05-AVM = 64Kx8
50 MHz max. Clock



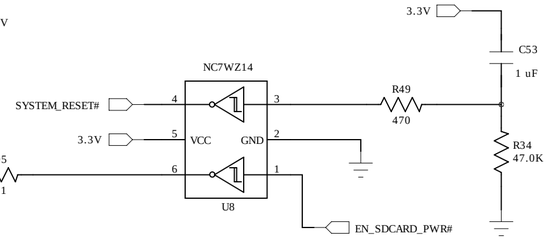
RTC



Micro SD Card Socket



Time constant
= 47 mS



Technologic Systems	Date March 22, 2015	
Title: TS-4200 Flash, NVRAM, RTC, Boot Flash		
Rev: E	Designer	Sheet 7 of 8

Two 100-pin Off-board Connectors

"POWER" pins supply all power to the module
Apply 3.6V to 5.5V to these pins

Current drain is 50mA to 400 mA

OFF_BD_RESET# is an Output
used to reset all peripherals

POWER_FAIL# must
not be driven high

EXT_RESET# is an Input
used to reboot the CPU

CN2 pin 27 should be connected
to CN2 pin 33 on the base board

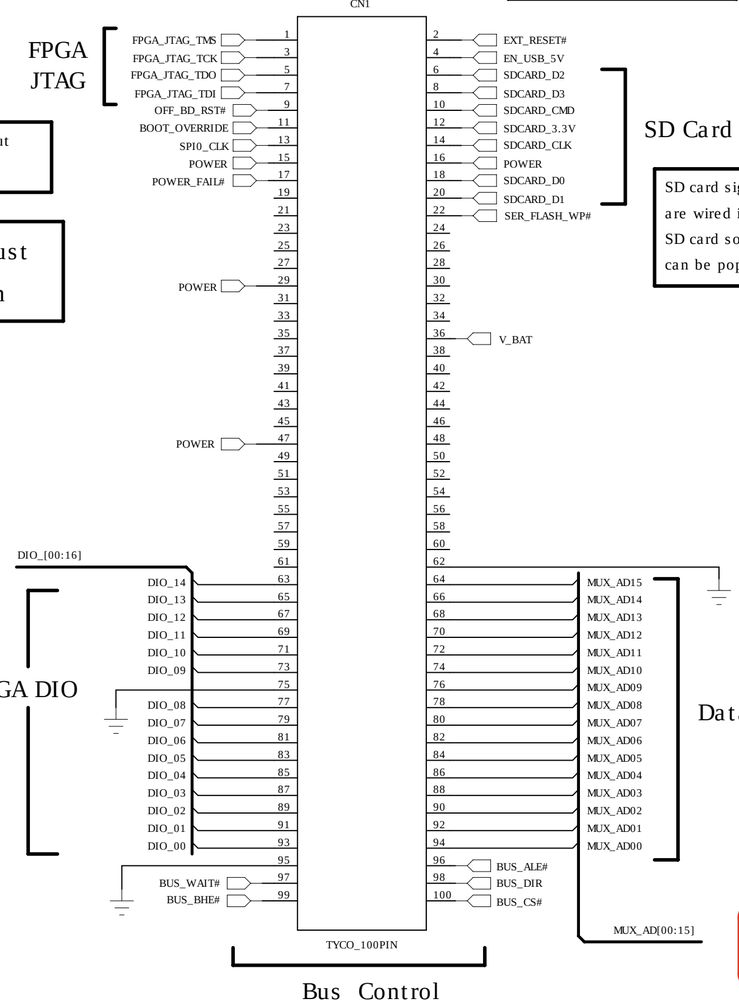
SD card signals on connector
are wired in parallel with
SD card socket. Only one
can be populated with SD card

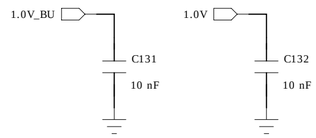
3.3V max load is 300 mA

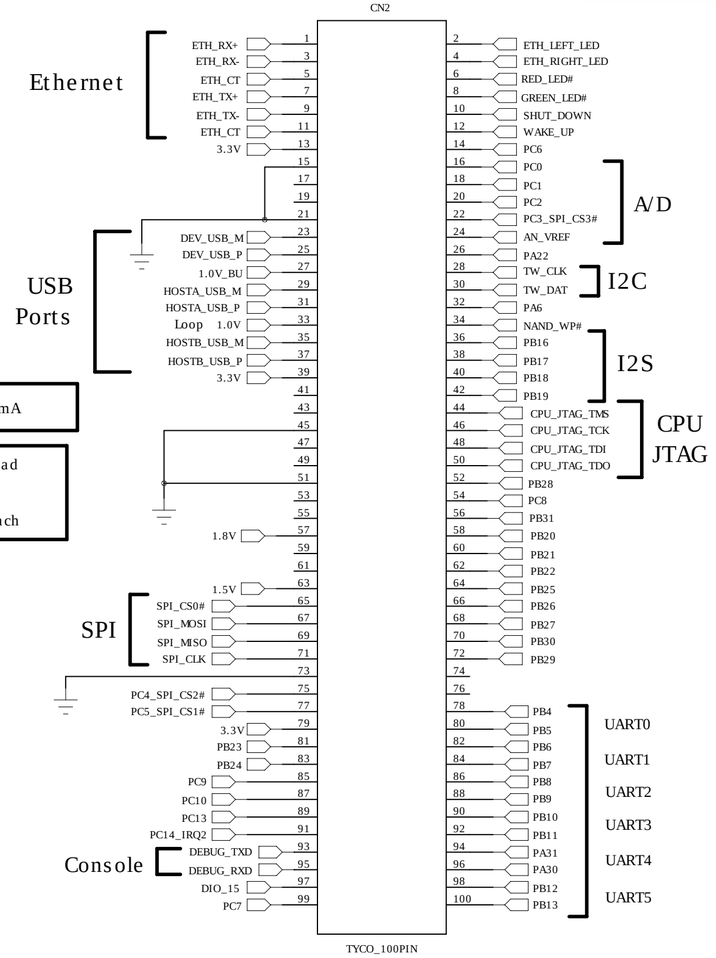
Maximum off-board load
on 1.8V, 1.5V and
1.0V pins is 10 mA each

⚠ All signals driving DIO on CN1 & CN2 must be powered by the 3.3V on CN2, or remain at 0V until the CN2 3.3V rail is > 3.0V

⚠ Pin 1 is the top left corner pin on the connector. All of the pins on the left are odd numbered. This may differ from the connector manufacture's datasheet.







⚠ Any I/O routed to a user accessible connector should have additional ESD protection placed on the carrier board.

Max. load on JTAG_Vcc
(CN2-79) is 20 mA

Boot Strap

Mode 2	Boots from
1	NAND Flash
0	SD Card

BUS_DIR = MODE2

MODE1 and MODE2 states
are latched prior to
OFF_BD_RESET# deasserted

MODE1 and MODE2
have PU resistors

Use 1.5K ohm resistor
to "OFF_BD_RESET#"
to set Mode pins "low"

Devices connected to this bus must never
drive it when BUS_CS# is deasserted
(must be off within 30 nS of deassertion)

Devices must pull the BUS_WAIT# line low
if they need more than 150 nS strobe

The data bus can not have more than
30 pF of off-board capacitive loading
May need data buffer chip for heavy loads

BUS_ALE# = Address Latch Enable
BUS_BHE# = Byte High Enable (for 16-bit cycles)

If Bus is not needed, the following
can be changed to DIO:
- Bus Control signals
- MUX_AD08 thru 15

Bus cycles use 11 address lines
AD0 thru AD10
This provides 1K address space
for 8-bit bus cycles (000-3FF)
and 1K for 16-bit cycles (400-7FF)

These DIO have 1.8V levels
PC4, PC5, PC6
PC7, PC8, PC9
PC10, PC13, PC14

All other DIO uses 3.3V levels

Technologic Systems	Date March 22, 2015	
Title: TS-4200 Off-board Connectors		
Rev: E	Designer	Sheet 8 of 8