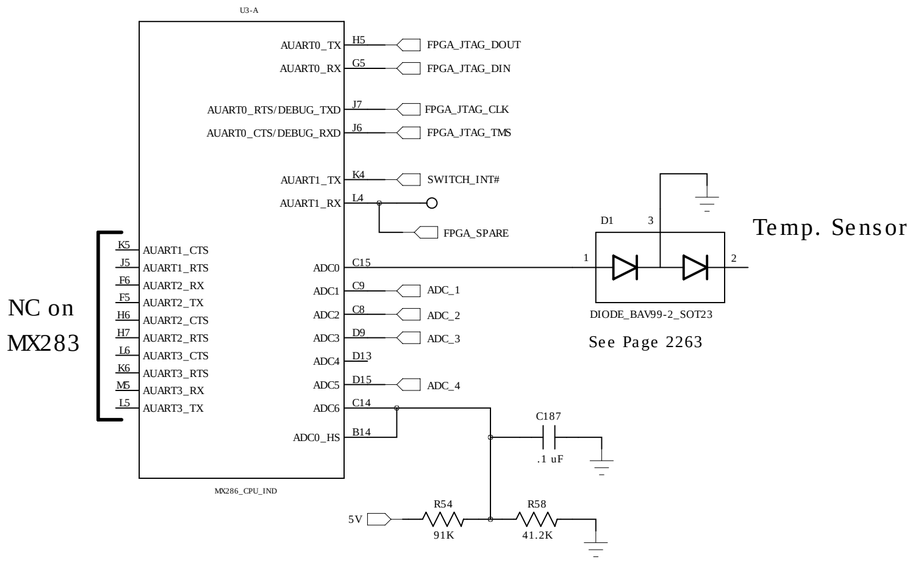
MX283 ARM9 CPU

UARTs, ADC



NC on MX283

Temp. Sensor

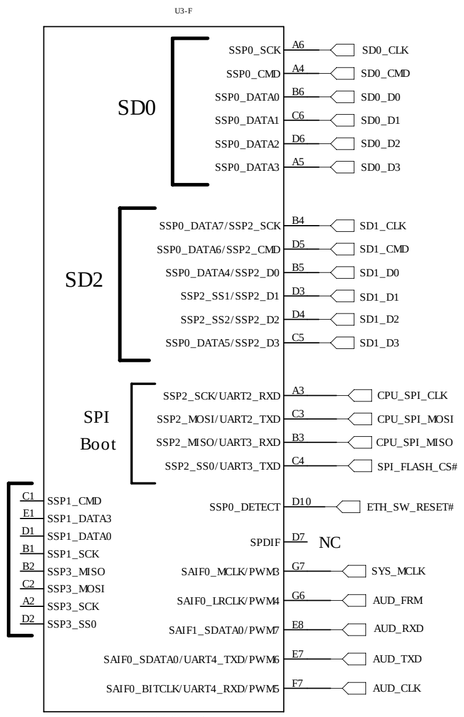
DIODE_BAV99-2_SOT23

See Page 2263

Audio

SD Card

SPI Boot



NC on MX283

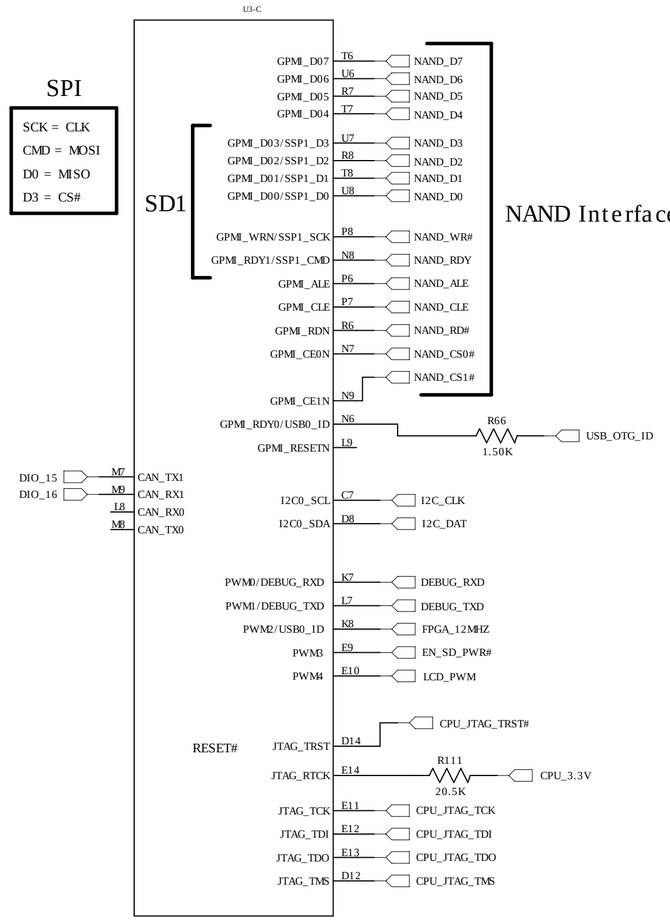
12 MHz default boot clock
Max SPI clock rate = 20 MHz

U3.D3 and U3.D4 are extra
2 data lines for SPI x4 read
Page 1313 of Data sheet

Page 1311 - Winbond SPI x2 and x4 supported
EVK schematic references a 8Mbit Winbond chip

NAND, PWM

JTAG, I2C



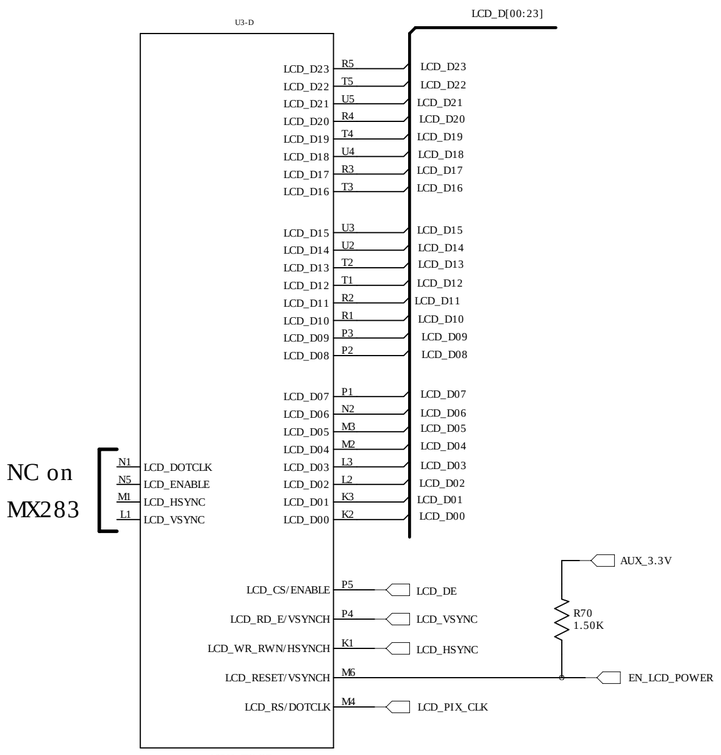
SPI

SCK = CLK
CMD = MOSI
D0 = MISO
D3 = CS#

NAND Interface

All JTAG have 47K internal PU except RTCK

LCD



NC on MX283

LCD_00 thru LCD_04
Control Boot Source

SPI = MSB 0 0 0 1 0 LSB

LCD_05 and 06 bias low
LCD_RS biased high
LCD_RS low = use OTP
See: EVK schematic, Page 15

F3 is EVK ETH_RESET#
F5, F6 are EVK USB_PWR_EN
E1 is EVK Eth_PWR_EN
C7 and D8 = EVK I2C
J5 is EVK USB_0_ID
K8 is EVK LCD PWM
K7 and L7 are EVK console

E10 is EVK SD1_PWR_EN

E9 is SD0 PWR_EN on both EVK and Green schematics

PWM outputs can be 24 MHz
divided by 16-bit integer
Allows clock 12MHz and lower

Rev.A Problems:

- Ethernet LEDs wrong !
- No CAN connected
- No A/D connected
- Add WiFi !
- Add low power modes ?
  - Pwr switch to PHY ?
- Remove FPGA ?

Technologic Systems	Date May 20, 2014	
Title: TS-4600 MX283 CPU		
Rev: B	Designer	Sheet 1 of 9

VDD4P2 is an output -- only feeds two 1.2K resistors

Reg VDD1P5 goes to nothing

Battery pin supplies current to charge battey

DCDC_BAT pin is power input for DCDC converters -- connect direct to battery

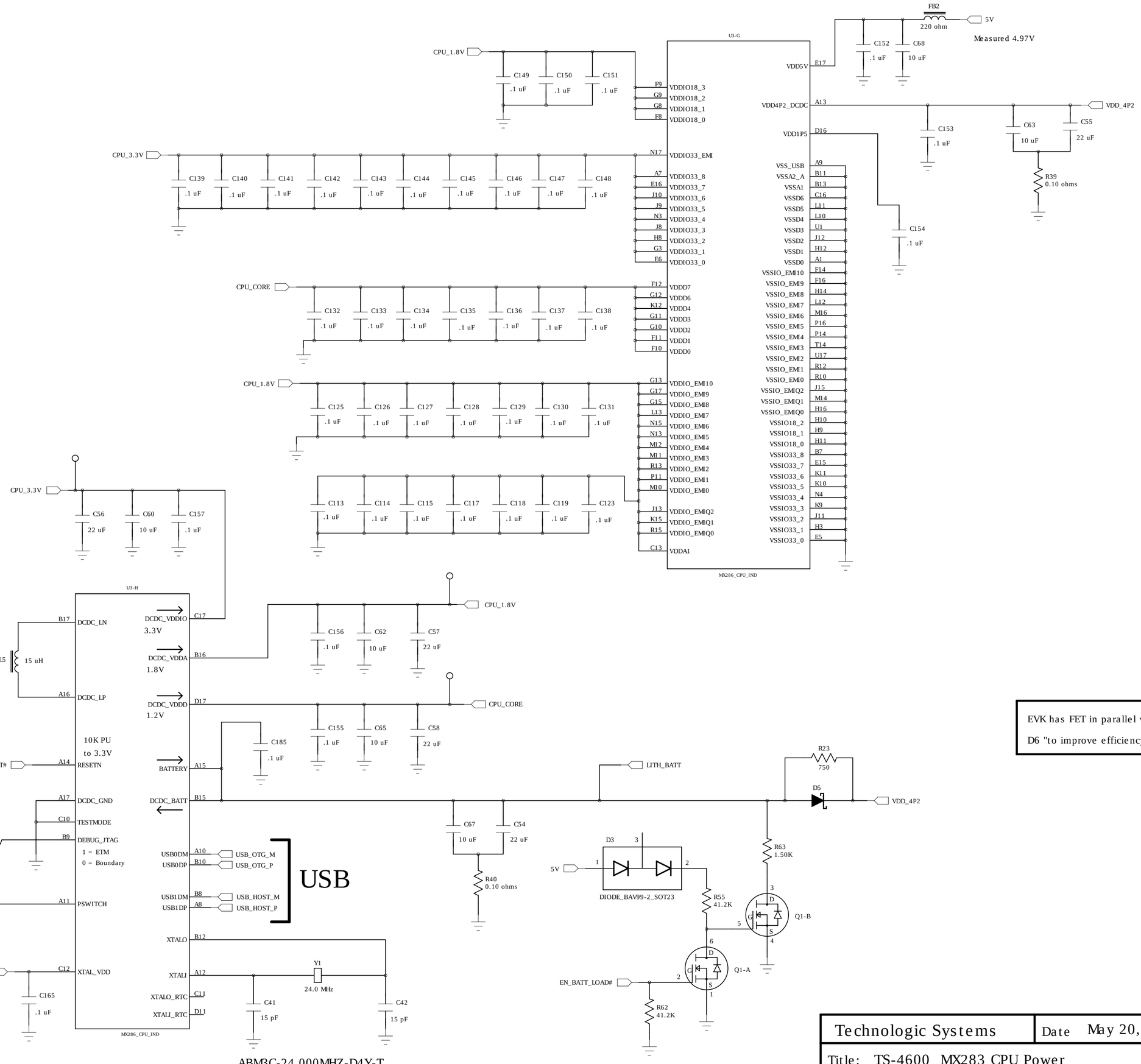
FPGA is fully functional when CPU Reset# deasserted

EVK has FET in parallel with D6 "to improve efficiency"

PSWITCH can be driven to 3.3V if a series 10K res is used

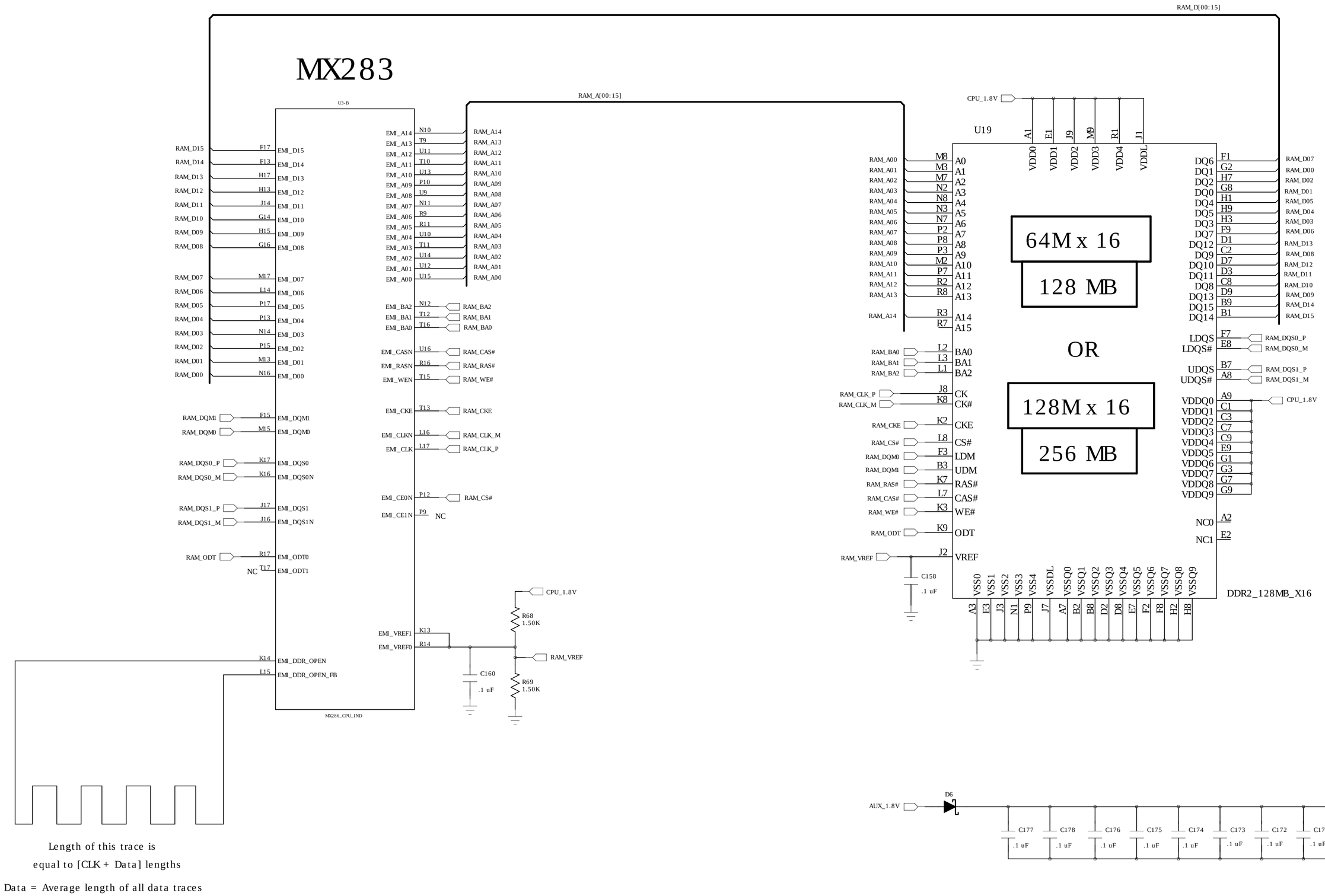
ABM3C-24.000MHZ-D4Y-T

CTS # 405C35E24M00000



Technologic Systems	Date May 20, 2014	
Title: TS-4600 MX283 CPU Power		
Rev: B	Designer	Sheet 2 of 9

DDR2 SDRAM (128 or 256 MByte)



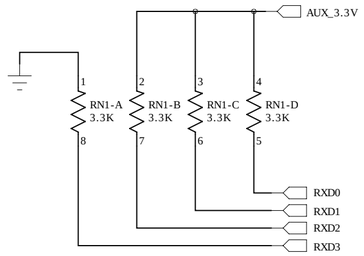
Length of this trace is
equal to [CLK + Data] lengths

Data = Average length of all data traces

Technologic Systems		Date May 20, 2014
Title: TS-4600 DDR2 RAM		
Rev: B	Designer	Sheet 3 of 9

10/100 Ethernet 4-Port Switch

"0111" = RMII MAC mode



Total 88E6020 100 Mbit

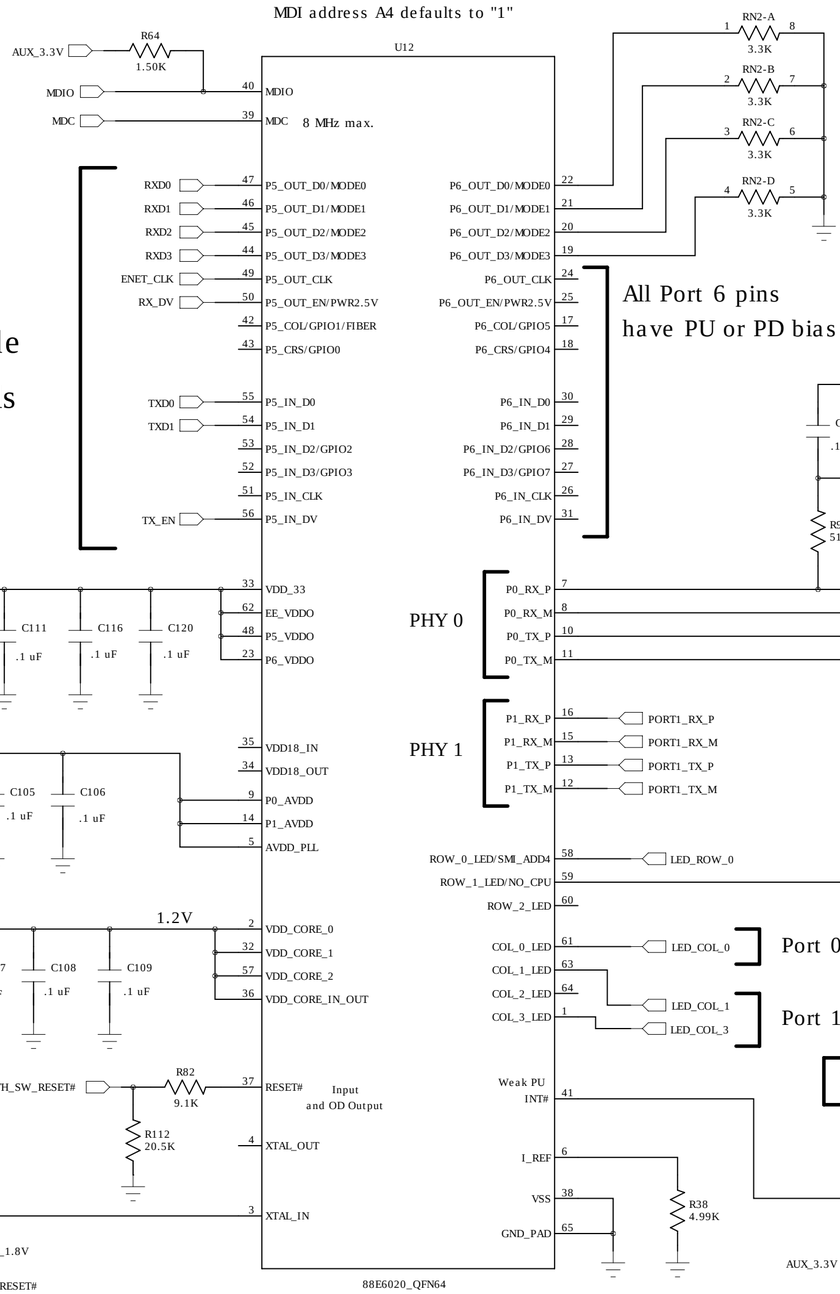
Current Drain includes
2 Ports with Mag CT

3.3V Rail = 20 mA
1.8V Rail = 80 mA
1.2V Rail = 62 mA

Power Down mode
42 mA on 1.2V rail
0 mA on other rails

MDI address A4 defaults to "1"

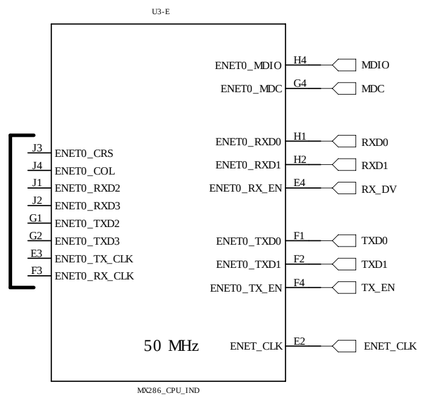
Strapped for
RMII MAC mode
with 3.3V Levels



All Port 6 pins
have PU or PD bias

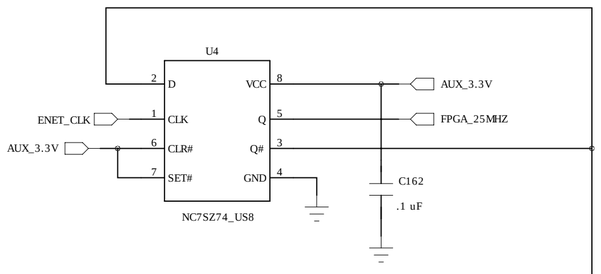
Pull-downs default P6
to port disabled mode

MX283

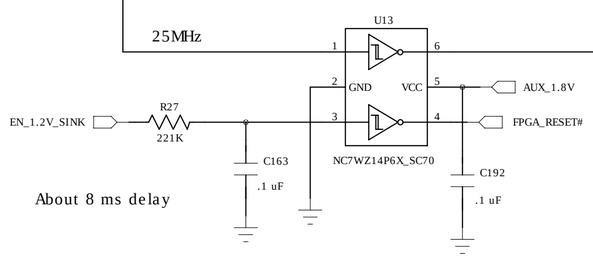


NC on
MX283

Page 883 - bit 18 controls
ENET_CLK direction

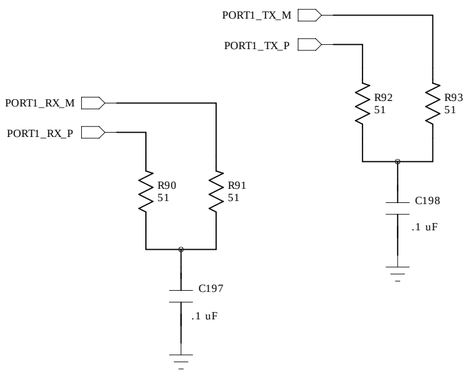


3.3V → 1.8V



About 8 ms delay

Requires Reset# asserted
for 10 ms after power

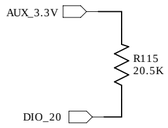


Auto MDIX is supported

Polarity Correction also supported

Technologic Systems	Date May 20, 2014	
Title: TS-4600 Ethernet Switch		
Rev: B	Designer	Sheet 4 of 9

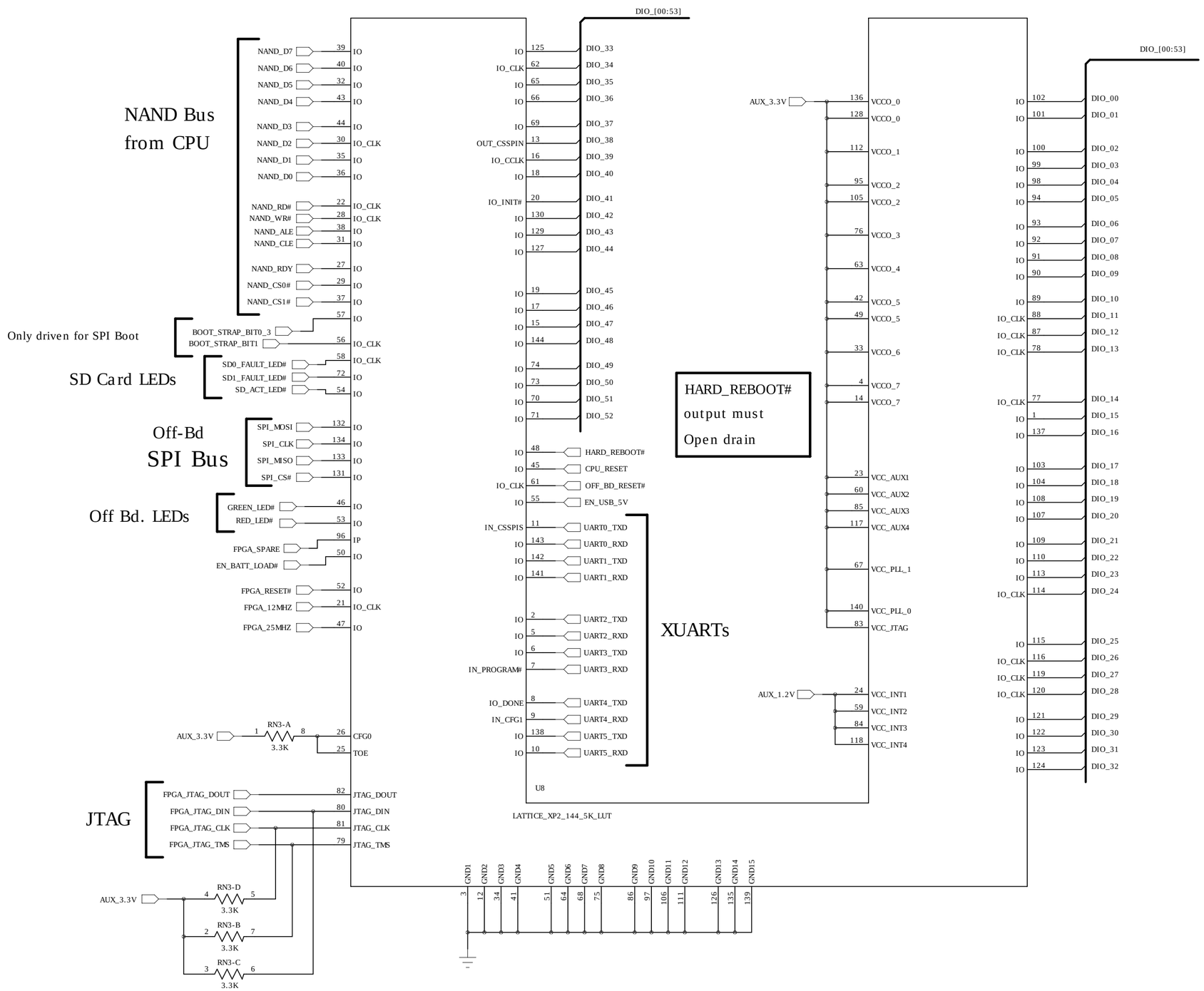
FPGA with 5K LUTs



DIO_20 is latched
when OFF_BD_RESET#
is deasserted
0 = SD Card Boot
1 = SPI Flash Boot

DIO_20, Red and Green LED
signals scan Base Bd. ID
DIO_05 returns values

FPGA_RESET# requires
special FPGA threshold set
This signal is 0-1.8V levels



HARD_REBOOT#
output must
Open drain

DIO_09 is sometimes
a Push switch input

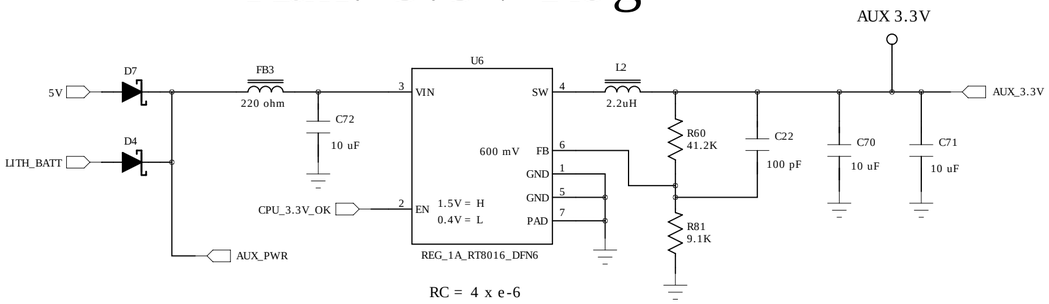
XP2-5 has:
5K or 8K LUTS 2 PLLs
9/12 blocks of 1Kx18 Block RAM
12 18x18 Multipliers
100 I/O with 144 pin package
"instant ON" = about 1.5 mS
input PLL clock = 10 MHz min

Pull-up and pull-down resistors
are 6 to 30K ohms

Page 37 of Data Sheet (Hot Socketing)
Power Supplies can be sequenced in any order
but must be monotonic
All I/O lines are tri-stated during power cycling

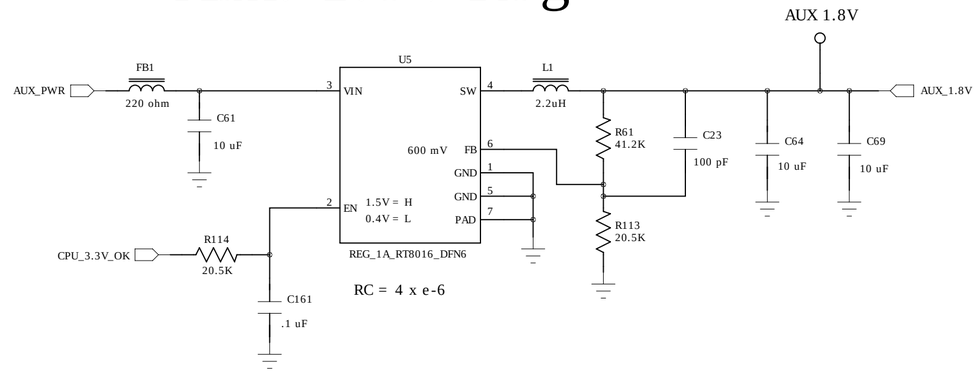
Technologic Systems	Date May 20, 2014	
Title: TS-4600 FPGA		
Rev: B	Designer	Sheet 5 of 9

Aux. 3.3V Reg



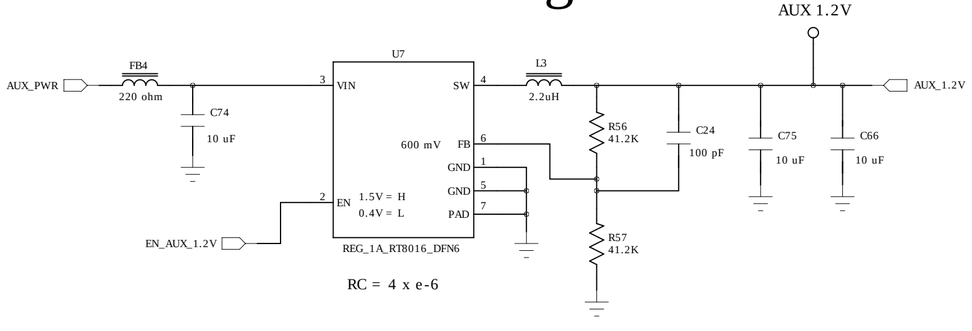
RC = 4 x e-6

Aux. 1.8V Reg



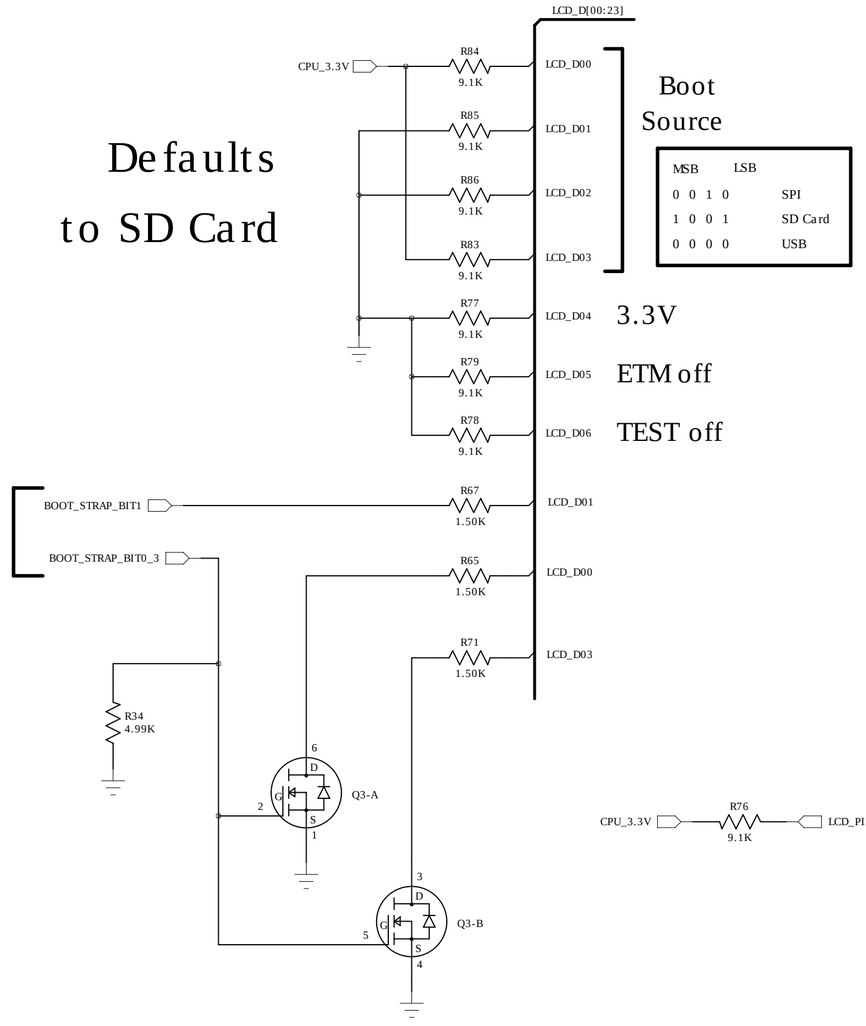
RC = 4 x e-6

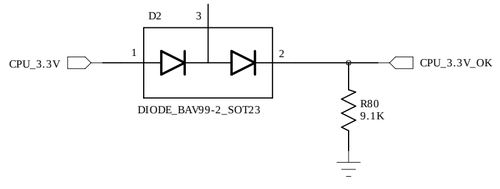
AUX 1.2V Reg.



RC = 4 x e-6

Boot Strap Bias Res.



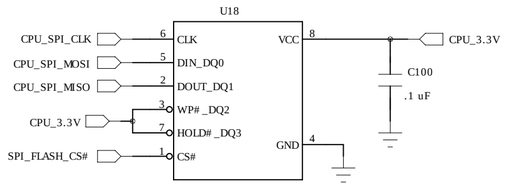


GND Test Point

Technologic Systems	Date May 20, 2014	
Title: TS-4600 Power Reg. and Boot Straps		
Rev: B	Designer	Sheet 6 of 9

MX283 SPI Boot and FPGA Config Flash

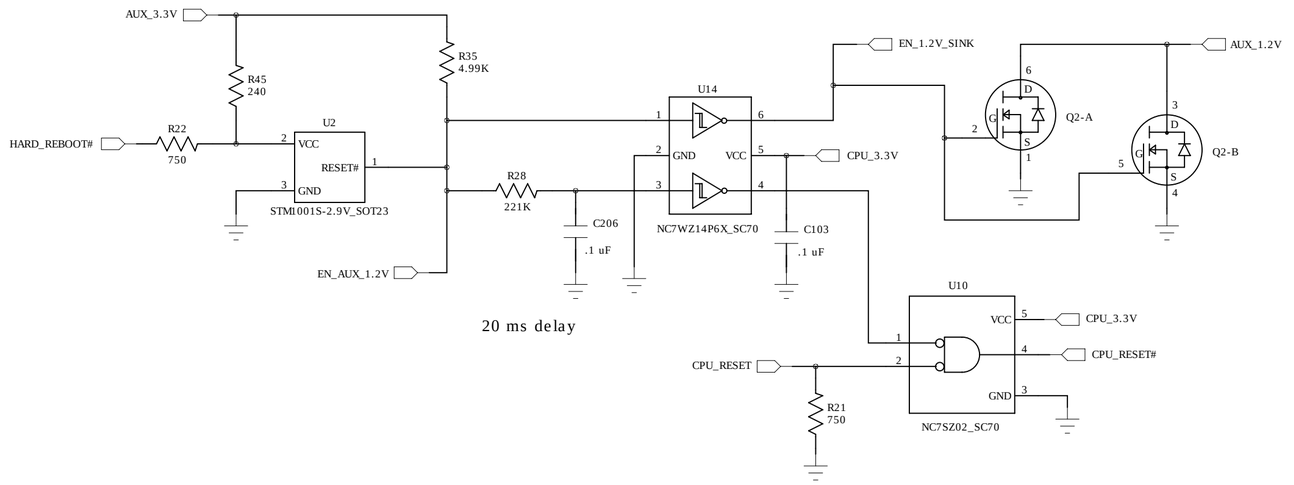
SPI Boot Flash



64 bytes of OTP

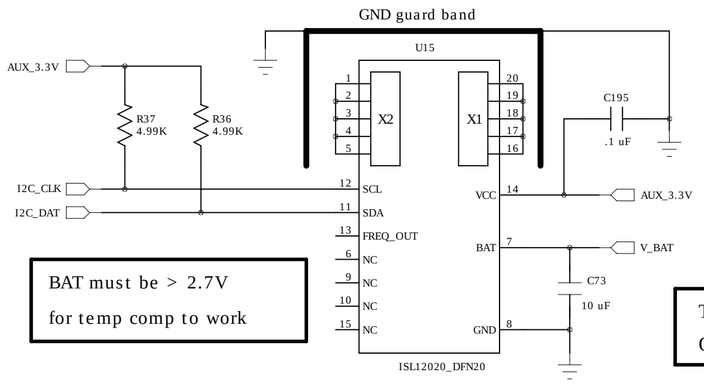
Not Populated ?

Reset Sequencer



20 ms delay

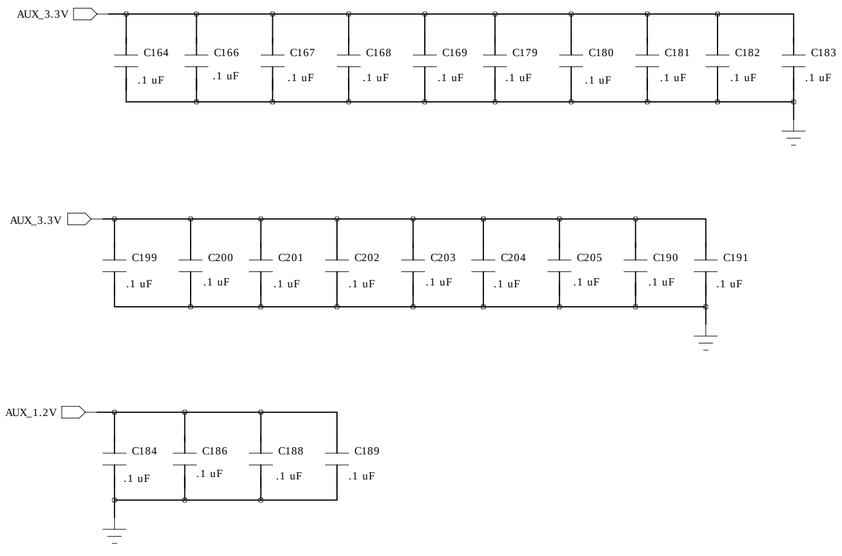
RTC and Temp. Sensor



BAT must be > 2.7V
for temp comp to work

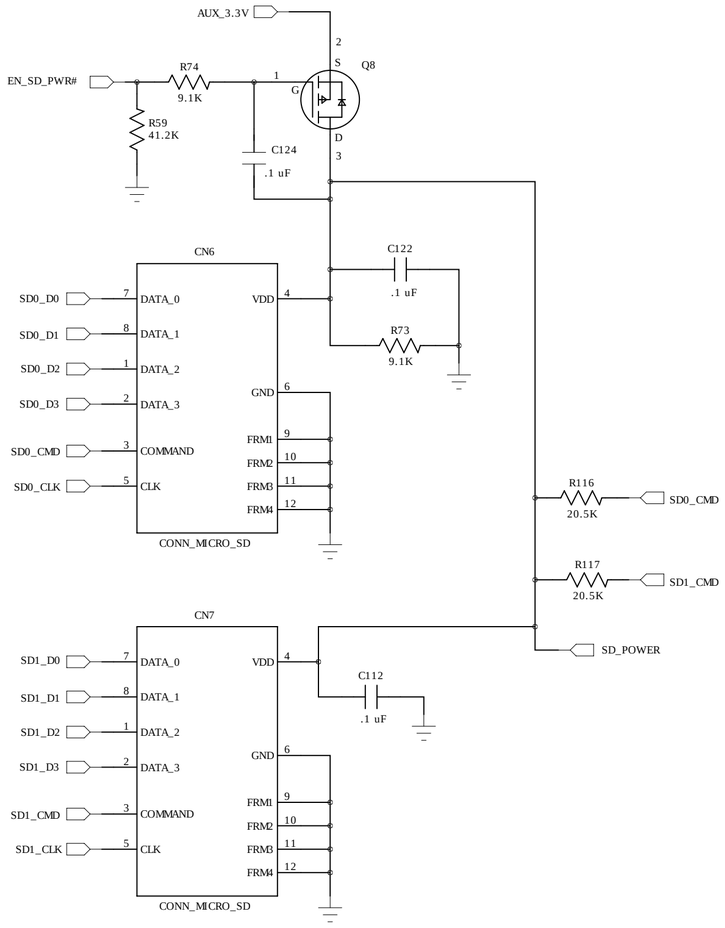
Temp takes 68 uA for 22 ms
Once every 1 or 10 min.

FPGA Bypass Caps

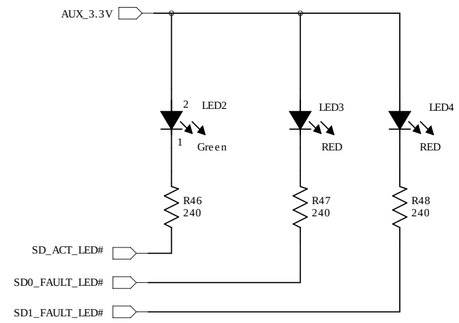


Technologic Systems	Date May 20, 2014	
Title: TS-4600 Boot Flash, FPGA Flash, RTC		
Rev: B	Designer	Sheet 7 of 9

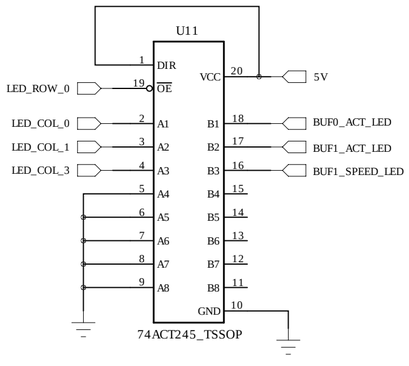
Micro SD Card Sockets



SD LEDs



Ethernet LED Buffer



Technologic Systems		Date May 20, 2014
Title: TS-4600 SD Card		
Rev: B	Designer	Sheet 8 of 9

Two 100-pin Off-board Connectors

"POWER" pins supply all power to the module
Apply 4.5V to 5.5V to these pins

Current drain is approximately 200 mA

REBOOT# is an Input
used to reboot the CPU

Do not drive active high
(use open drain)

OFF_BD_RESET# is an Output
used to reset all peripherals

Left

CN1

FPGA JTAG: FPGA_JTAG_TMS 1, FPGA_JTAG_CLK 3, FPGA_JTAG_DOUT 5, FPGA_JTAG_DIN 7

OFF_BD_RESET# 9

NC 11, NC 13, 5V 15, NC 17

LCD_D08 19, LCD_D09 21, LCD_D10 23, LCD_D11 25, LCD_D12 27

5V 29

C102 .1 uF, C101 .1 uF

LCD_D13 31, LCD_D14 33, LCD_D15 35, LCD_D16 37, LCD_D17 39, LCD_D18 41, LCD_D19 43, LCD_D20 45

5V 47

LCD_PIX_CLK 49, LCD_HSYNC 51, LCD_VSYNC 53, LCD_DE 55, LCD_PWM 57

DIO_[00:53]

FPGA DIO: DIO_50 59, DIO_49 61, DIO_14 63, DIO_13 65, DIO_12 67, DIO_11 69, DIO_10 71, DIO_09 73, DIO_08 75, DIO_07 77, DIO_06 79, DIO_05 81, DIO_04 83, DIO_03 85, DIO_02 87, DIO_01 89, DIO_00 91, 93, 95, DIO_17 97, DIO_18 99

HARD_REBOOT# 2, EN_USB_5V 4

Off-Bd SD Card: SD1_D2 6, SD1_D3 8, SD1_CMD 10, SD_POWER 12, SD1_CLK 14, 5V 16, SD1_D0 18, SD1_D1 20

LCD_D00 22, LCD_D01 24, LCD_D02 26, LCD_D03 28, LCD_D04 30, LCD_D05 32, V_BAT 34, LCD_D06 36, LCD_D07 38, LCD_D21 40, LCD_D22 42, LCD_D23 44, EN_LCD_POWER 46, 48, LITH_BATT 50

DIO_52 54, DIO_51 56

16 bit Data Bus or DIO: DIO_37 58, DIO_36 60, DIO_35 62, DIO_34 64, DIO_33 66, DIO_32 68, DIO_31 70, DIO_30 72, DIO_29 74, DIO_28 76, DIO_27 78, DIO_26 80, DIO_25 82, DIO_24 84, DIO_23 86, DIO_22 88, DIO_21 90, DIO_20 92, DIO_19 94

DIO_[00:53]

CONN_TYCO_100PIN_SBC

All signals driving DIO on CN1 & CN2 must be powered by the 3.3V on CN2, or remain at 0V until the CN2 3.3V rail is > 3.0V

Must have 10 nF Capacitor
very near CN2 and GND
for all "quiet" signals
(between diff pairs)

Pin 1 is the top left corner pin on the connector. All of the pins on the left are odd numbered. This may differ from the connector manufacture's datasheet.

Right

CN2

Primary Ethernet: PORT1_RX_P 1, PORT1_RX_M 3, AUX_1.8V 5, PORT1_TX_P 7, PORT1_TX_M 9, AUX_1.8V 11

13, 15, 17, 19, 21

NC 23, NC 25, NC 27

3.3V rail can supply up
to 400 mA to base board

USB Ports: USB_HOST_M 29, USB_HOST_P 31, CPU_CORE 33, USB_OTG_M 35, USB_OTG_P 37

AUX_3.3V 39

C196 .1 uF

ADC_2 41, CPU_JTAG_TRST# 43

45, 47, 49, 51

AUX_1.8V 53

SPI or DIO: SPI_CS# 55, SPI_MOSI 57, SPI_MISO 59, SPI_CLK 61

CPU JTAG: CPU_3.3V 63

65, 67, 69, 71, 73, 75

1V 77, CPU_PSWITCH 79, ADC_3 81, ADC_4 83

Console: DEBUG_TXD 85, DEBUG_RXD 87, DIO_15 89, DIO_16 91

BUF1_ACT_LED 2, BUF1_SPEED_LED 4, RED_LED# 6, GREEN_LED# 8

BUF0_ACT_LED 10, ADC_1 12

2nd Ethernet Port: PORT0_RX_P 14, PORT0_RX_M 16, AUX_1.8V 18, PORT0_TX_P 20, PORT0_TX_M 22

24

I2C: I2C_CLK 26, I2C_DAT 28

DIO_[00:53]

DIO_48 30

I2S or DIO: SYS_MCLK 32, AUD_CLK 34, AUD_FRM 36, AUD_TXD 38, AUD_RXD 40

CPU JTAG: CPU_JTAG_TMS 42, CPU_JTAG_TCK 44, CPU_JTAG_TDI 46, CPU_JTAG_TDO 48

DIO_47 50

SYS_MCLK 52

DIO_46 54, DIO_45 56, DIO_44 58, DIO_43 60, DIO_42 62, DIO_41 64, DIO_40 66, DIO_39 68, DIO_38 70

USB_OTG_ID 72

74

Serial Ports or DIO: UART0_TXD 76, UART0_RXD 78, UART1_TXD 80, UART1_RXD 82, UART2_TXD 84, UART2_RXD 86, UART3_TXD 88, UART3_RXD 90, UART4_TXD 92, UART4_RXD 94, UART5_TXD 96, UART5_RXD 98

CONN_TYCO_100PIN_SBC

AUX_1.8V

C104 .1 uF near CN2-20

If Bus is not needed, all Bus
signals can be changed to DIO

Any I/O routed to a user accessible connector should have additional ESD protection placed on the carrier board.

Devices connected to this bus must never drive it when BUS_CS# is deasserted

(must be off within 30 nS of deassertion)

Devices must pull the BUS_WAIT# line low if they need more than 150 nS strobe

Technologic Systems		Date May 20, 2014
Title: TS-4600 100 pin Connectors		
Rev: B	Designer	Sheet 9 of 9