Documentation

XOPP1
NC
ASSEMBLY_OPTIONS

Changes from Rev.B to Rev.C

Removed two DDR2 x8 RAMs (Comm Temp)

Added one DDR3 x16 RAM (Comm Temp)

Changed RAM 1.8V power supply
from 1.8V to 1.5V
and used Marvell switching reg.

Added Termination power rail (U17)
and termination resistors

TS-4700 Rev.C BOMs

There are two BOM types:

One with a 5K LUT FPGA TSPN 35-3100-9

One with a 8K LUT FPGA TSPN 35-6142-7

OPT1 = UT-4700-256-256XF is 5K LUT

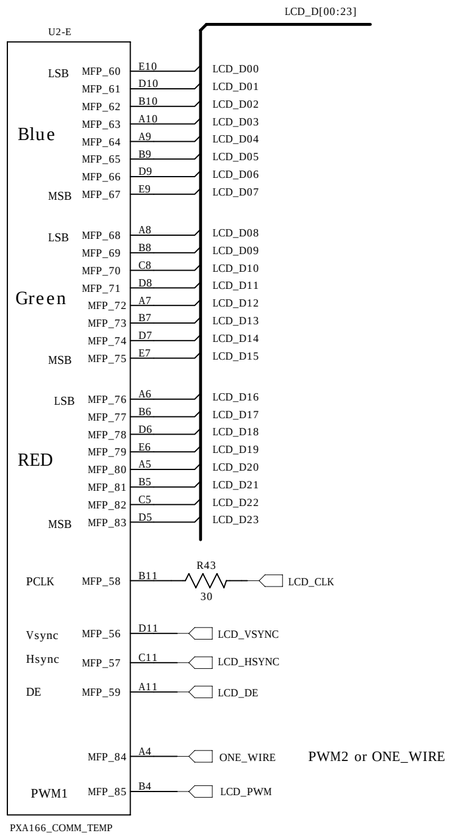
Opt2 = UT-4700-256-256XF-8K = 8K LUT

R56 not populated on any BOM

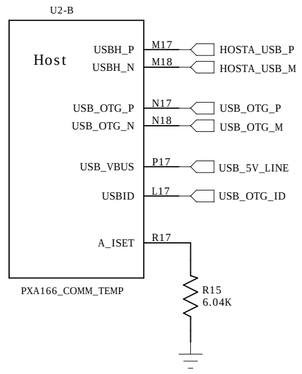
Technologic Systems	Date Dec. 30, 2015	
Title: TS-4700 Documentation		
Rev: C	Designer RLM	Sheet 1 of 11

PXA166 800 MHz CPU

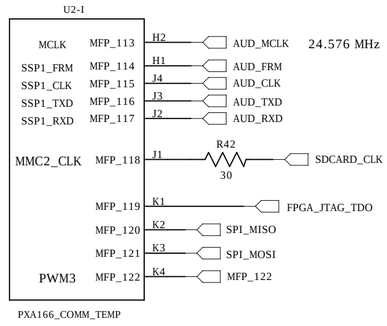
LCD



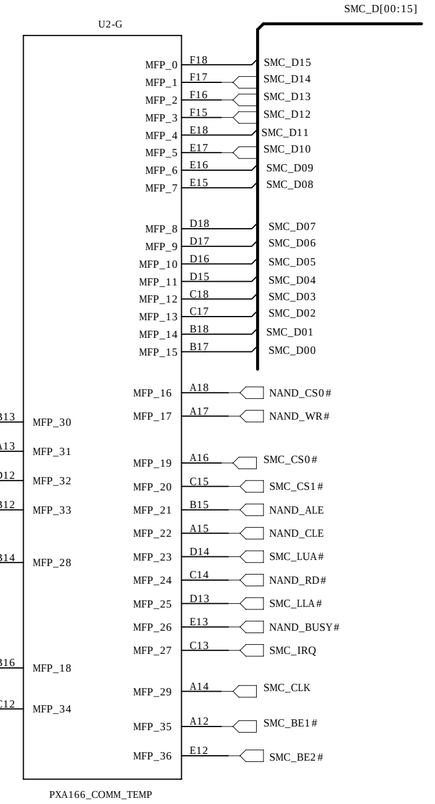
USB Ports



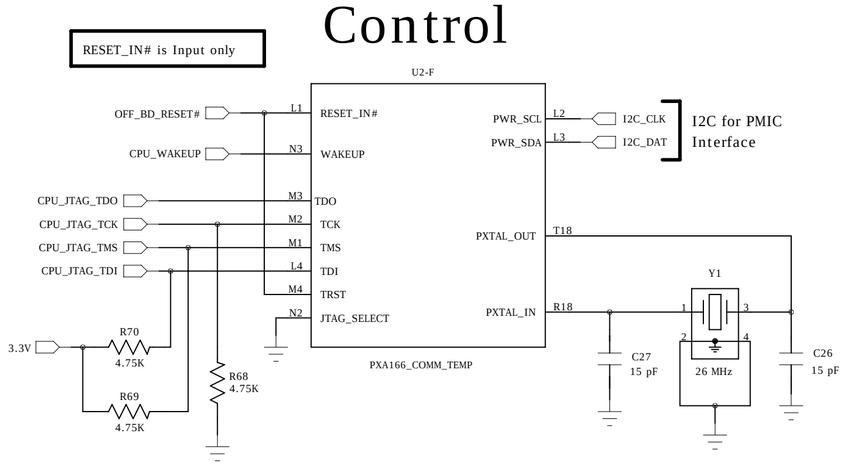
I2S



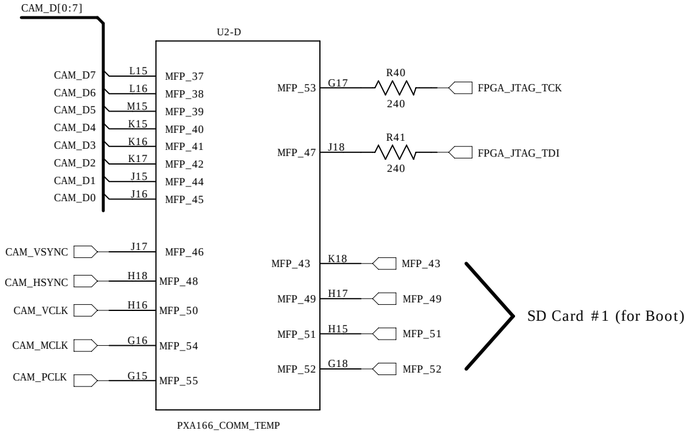
SMC Bus



Control



Camera



Technologic Systems	Date Dec. 30, 2015	
Title: TS-4700 Marvell PXA166 or PXA168		
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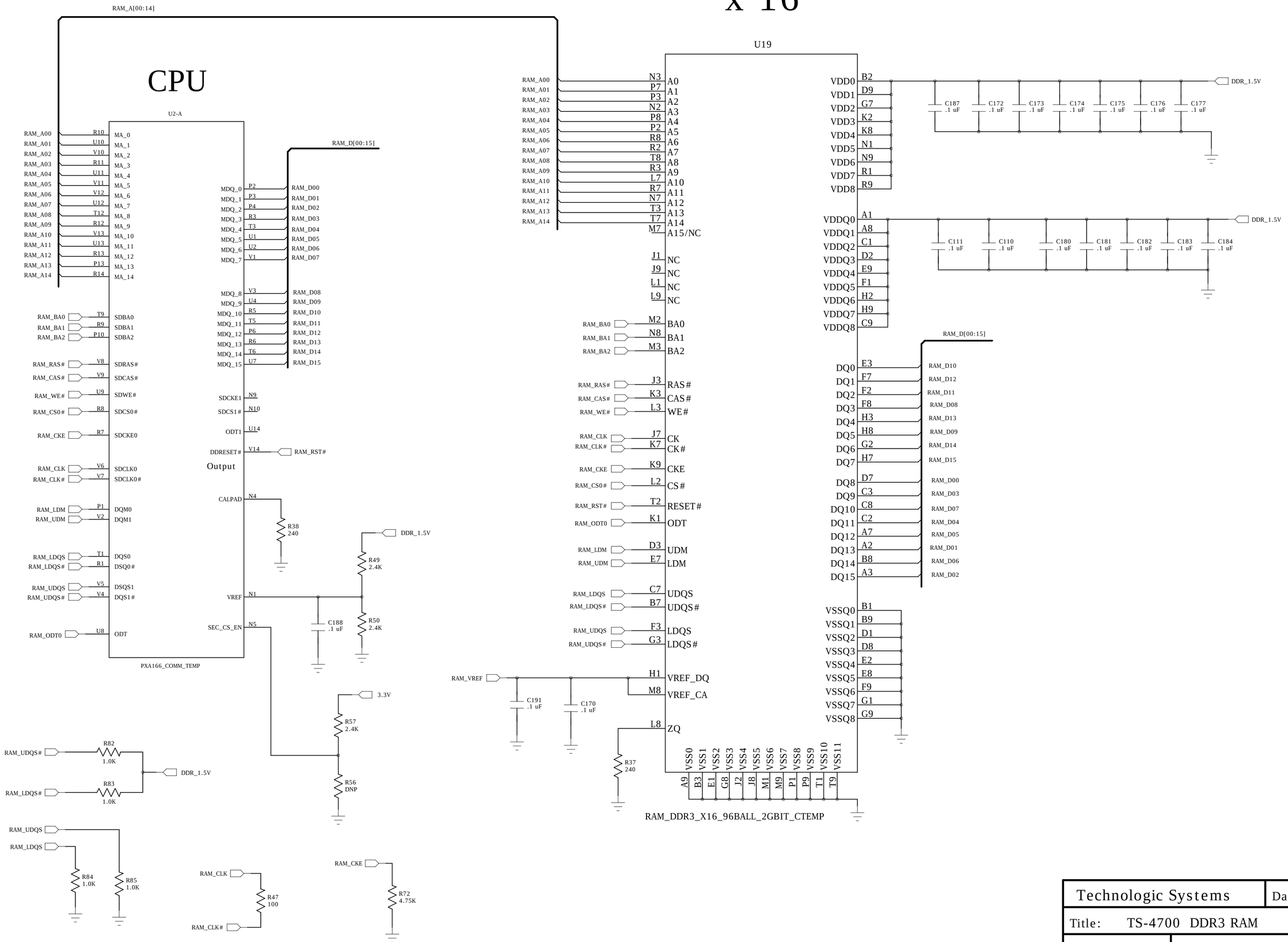
DDR3 SDRAM

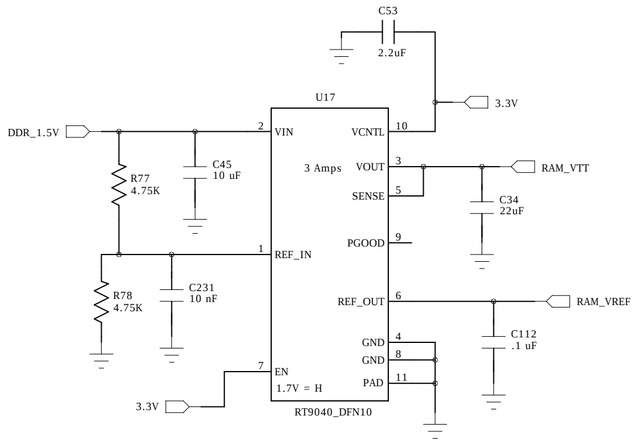
256 MB

x 16

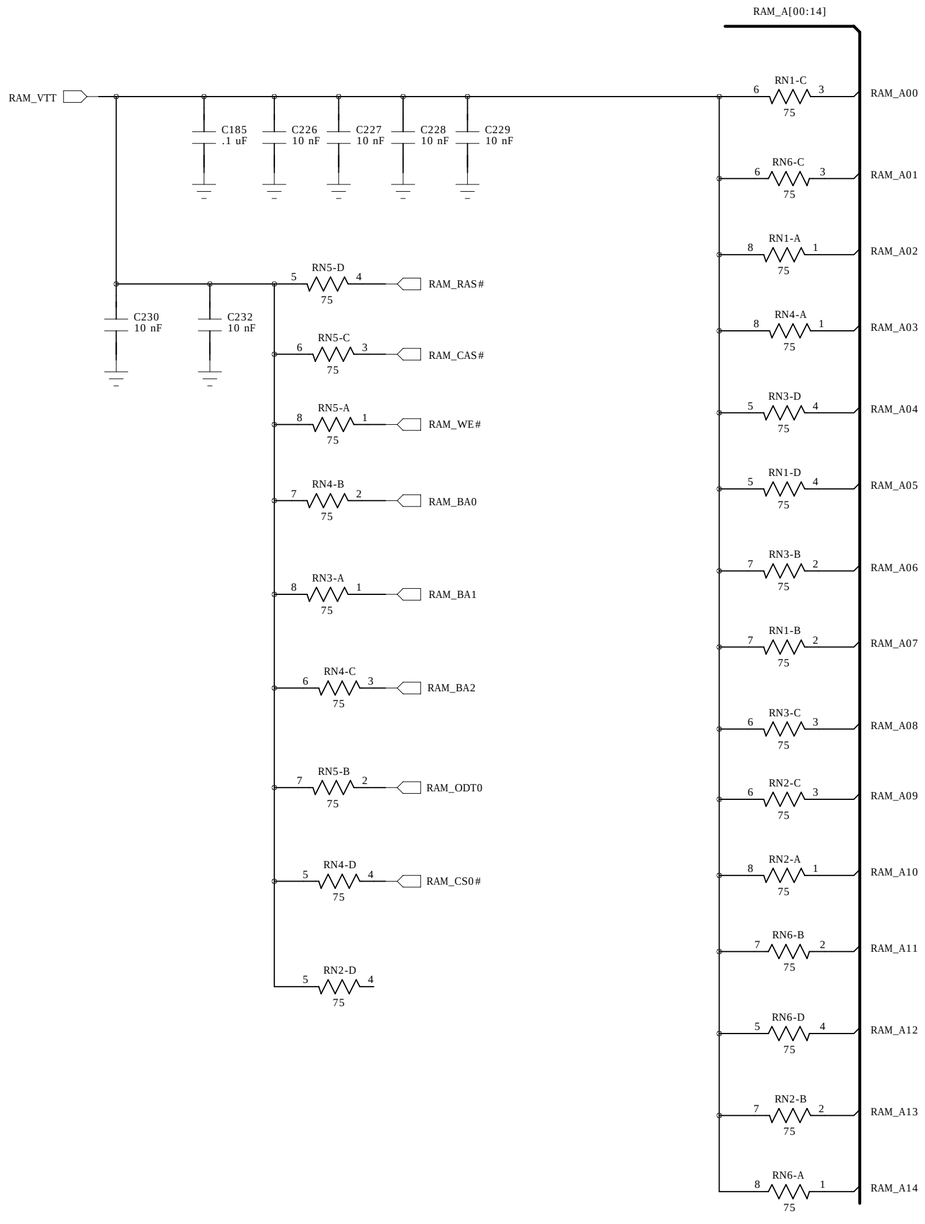


Technologic Systems	Date Dec. 30, 2015	
Title: TS-4700 DDR3 RAM		
Rev: C	Designer	Sheet 4 of 11

DDR3 RAM Termination Power Supply



Termination Resistors



Technologic Systems	Date Dec. 30, 2015	
Title: TS-4700 RAM Termination		
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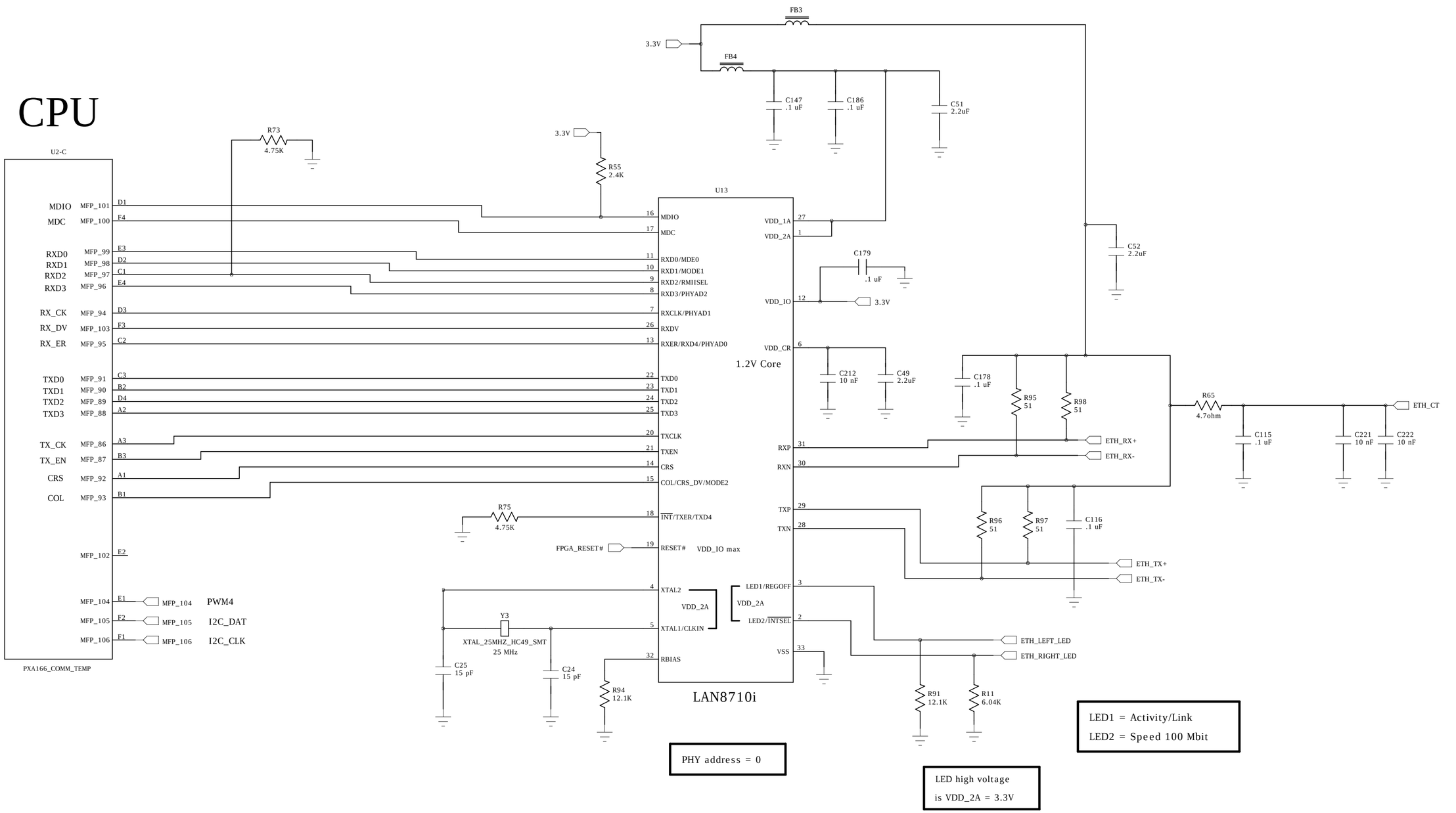
10/100 Ethernet

CPU

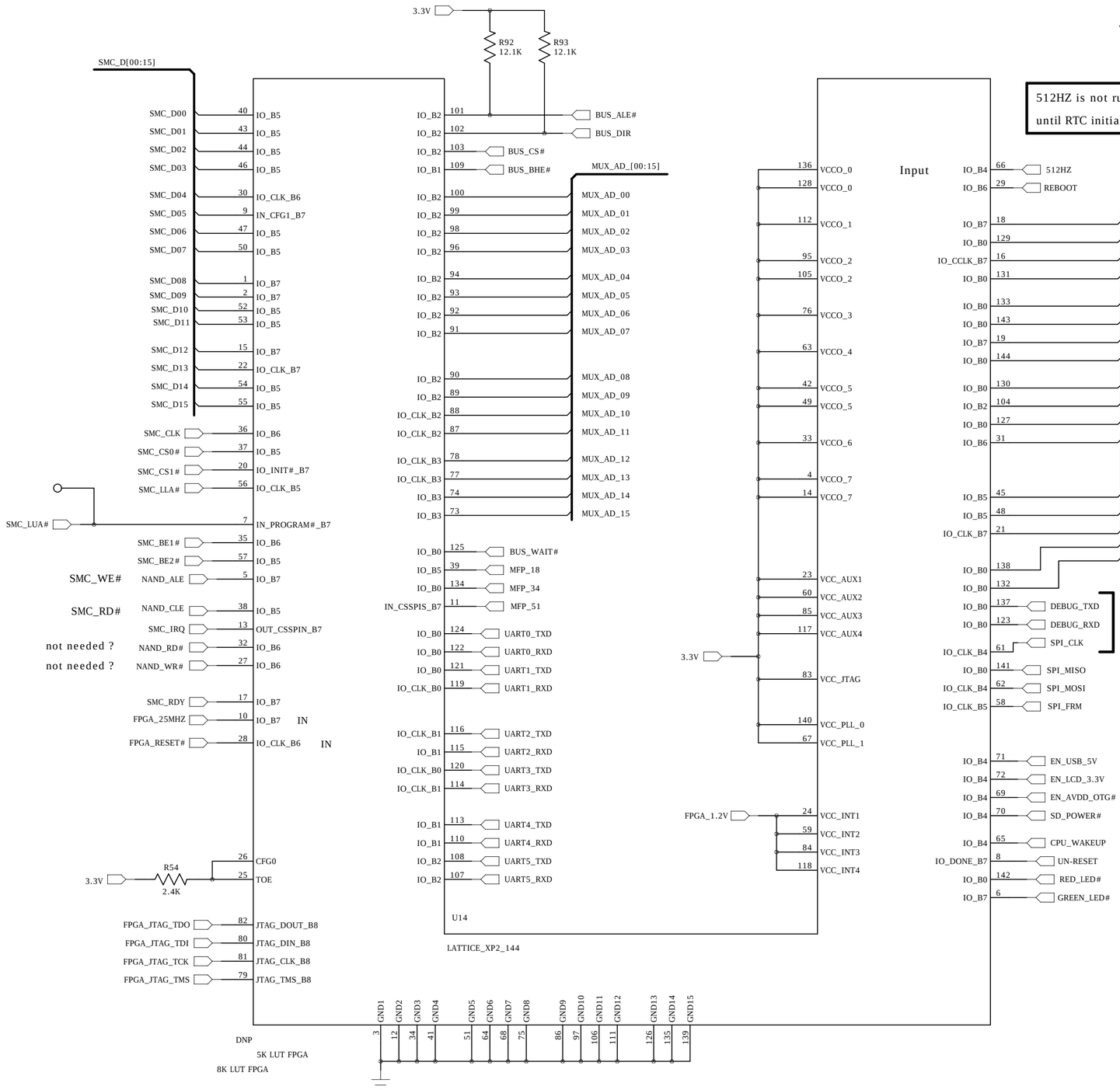


Technologic Systems	Date Dec. 30, 2015	
Title: TS-4700 Ethernet		
Rev: C	Designer RLM	Sheet 6 of 11

FPGA with 5000 LUTs

Boot Strap

Mode 2	TS-4700 Boots from
1	NAND Flash
0	SD Card



USB Power

Reset Latch

FPGA 1.2V Reg.

Technologic Systems	Date Dec. 30, 2015	
Title: TS-4700 FPGA		
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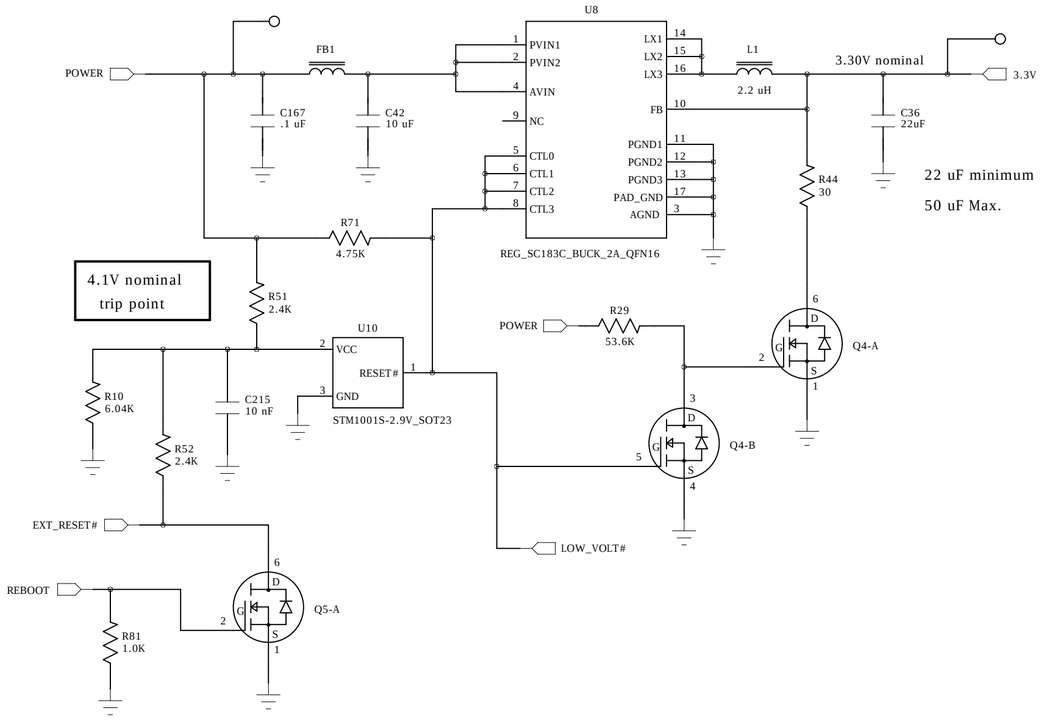
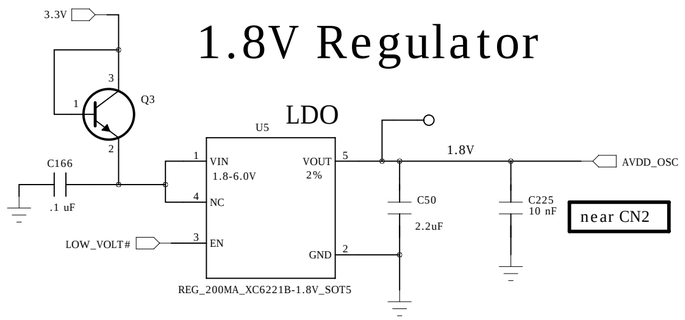
POWER

#1 3.3V Power Supply

up to 2000 mA

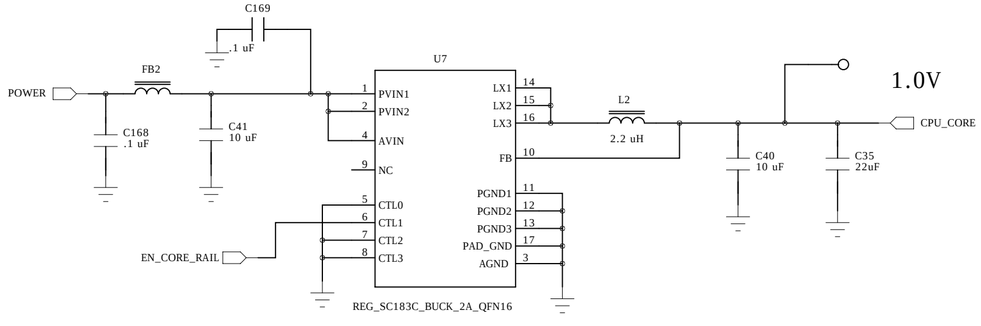


#2 Analog 1.8V Regulator

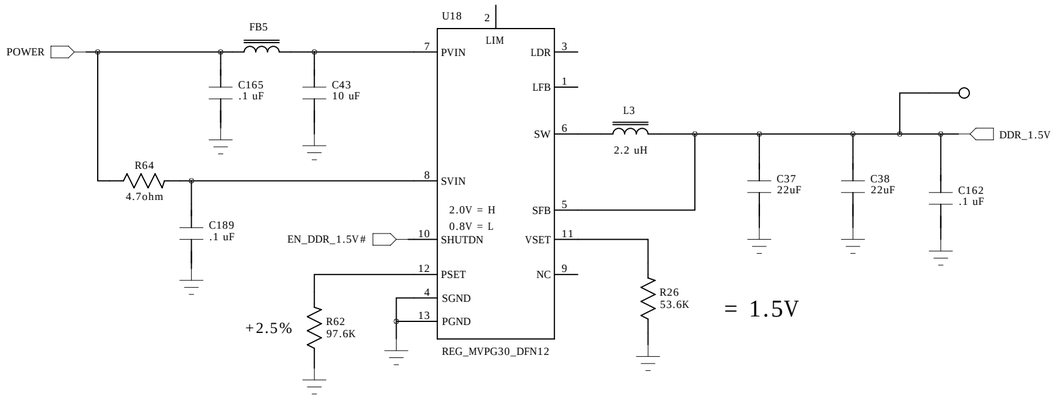


GND

#3 CPU Core Supply

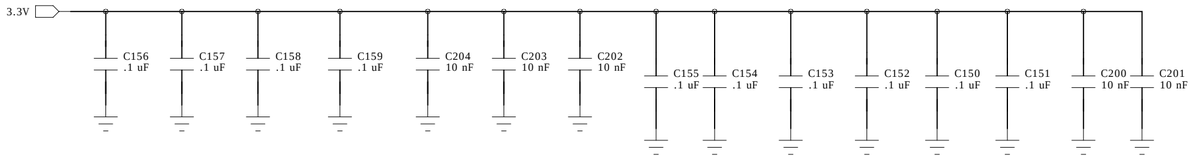


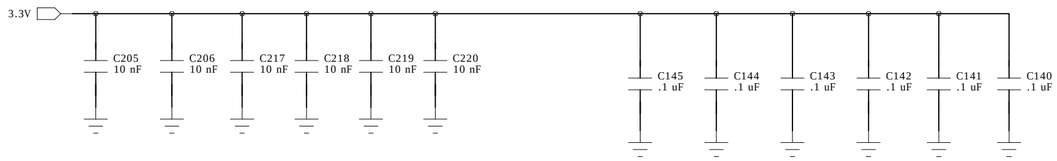
#4 DDR3 1.5V Reg.

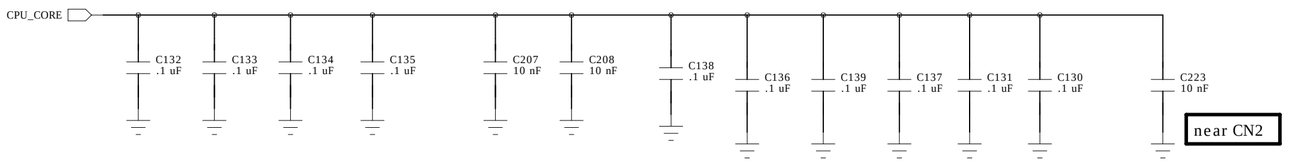


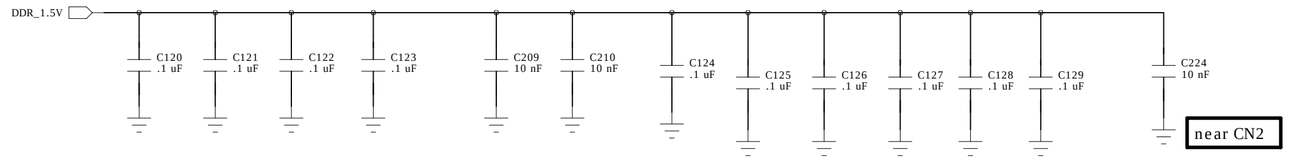
Technologic Systems	Date Dec. 30, 2015	
Title: TS-4700 Power Supplies		
Rev: C	Designer	Sheet 8 of 11

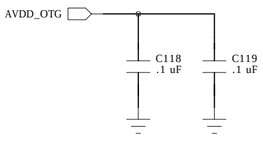
CPU Power



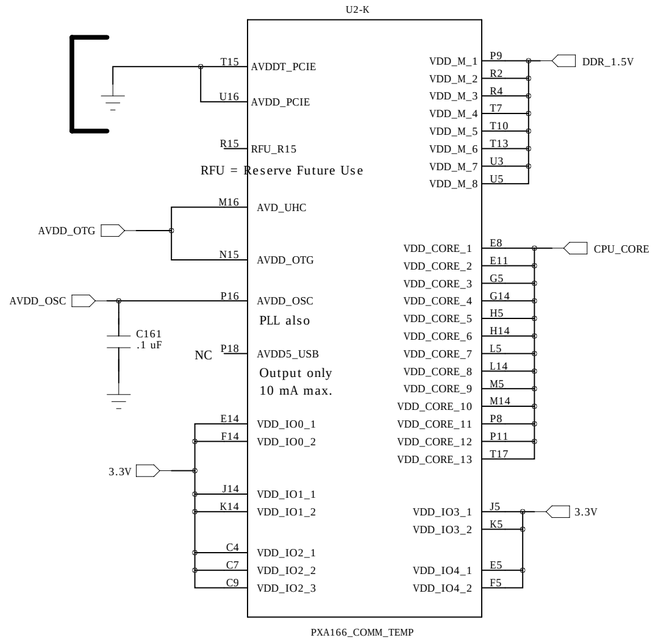




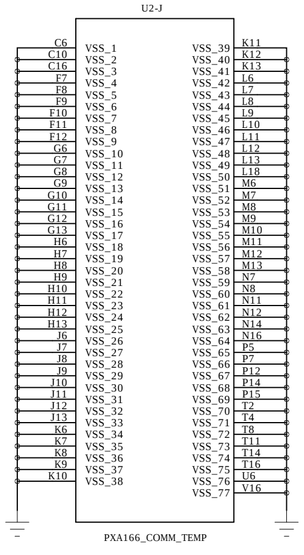




CPU

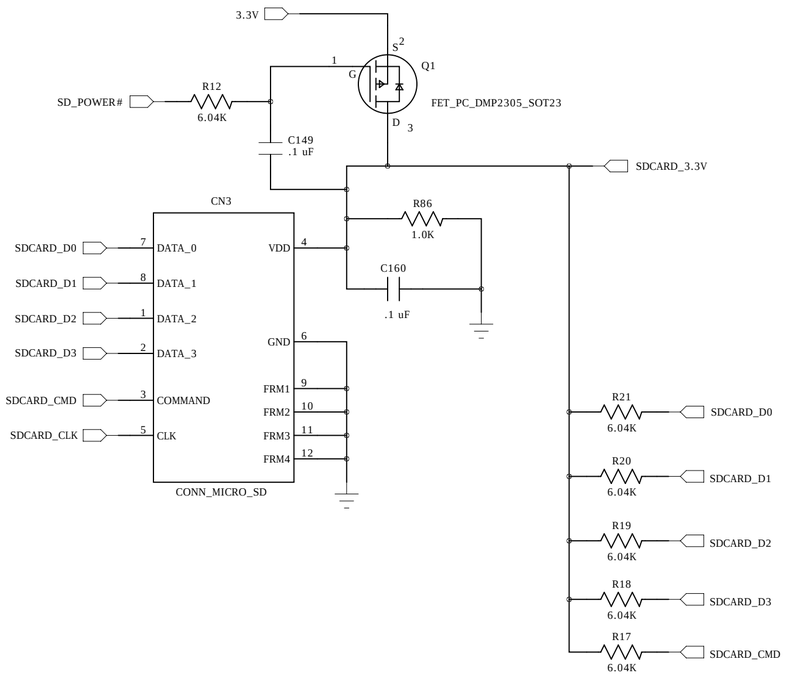


CPU

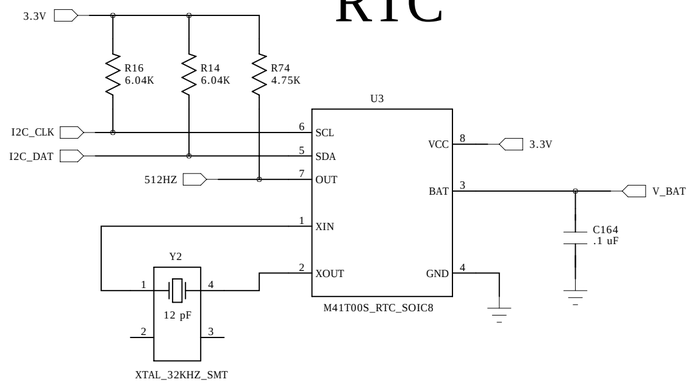


Technologic Systems	Date Dec. 30, 2015	
Title: TS-4700 CPU Power and Bypass caps		
Rev: C	Designer	Sheet 9 of 11

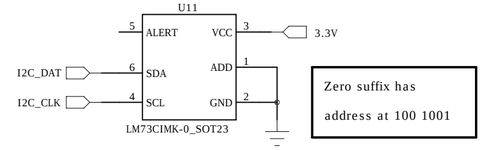
Micro SD Card Socket



RTC



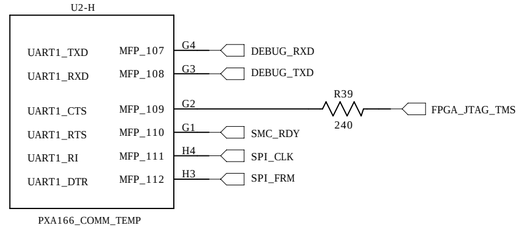
Temp Sensor



LM73CIMK-0

CPU

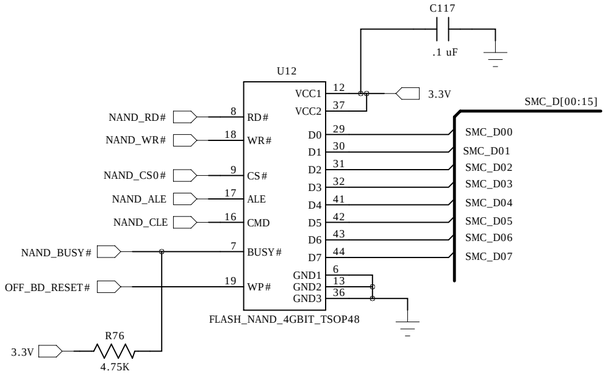
UART 1



(Console)

512 Mbyte

NAND Flash



Technologic Systems	Date Dec. 30, 2015	
Title: TS-4700 SD card, NAND, RTC		
Rev: C	Designer	Sheet 10 of 11

Two 100-pin Off-board Connectors

"POWER" pins supply all power to the module
Apply 4.5V to 5.5V to these pins

Current drain is approximately 400 mA

EXT_RESET# is an Input
used to reboot the CPU

Do not drive active high
(use open drain)

⚠ All signals driving DIO on CN1 & CN2 must be powered by the 3.3V on CN2, or remain at 0V until the CN2 3.3V rail is > 3.0V

⚠ Pin 1 is the top left corner pin on the connector. All of the pins on the left are odd numbered. This may differ from the connector manufacture's datasheet.

Left

CN1

FPGA JTAG: FPGA_JTAG_TMS 1, FPGA_JTAG_TCK 3, FPGA_JTAG_TDO 5, FPGA_JTAG_TDI 7, OFF_BD_RESET# 9

OFF_BD_RESET# is an Output
used to reset all peripherals

NC 11, NC 13, POWER 15, POWER_FAIL# NC 17

LCD_D08 19, LCD_D09 21, LCD_D10 23, LCD_D11 25, LCD_D12 27, 29

POWER — C146 .1 uF, C148 .1 uF

LCD_D13 31, LCD_D14 33, LCD_D15 35, LCD_D16 37, LCD_D17 39, LCD_D18 41, LCD_D19 43, LCD_D20 45, POWER 47, LCD_CLK 49, LCD_HSYNC 51, LCD_VSYNC 53, LCD_DE 55, LCD_PWM 57, 59, 61

DIO_[00:16]

FPGA DIO: DIO_14 63, DIO_13 65, DIO_12 67, DIO_11 69, DIO_10 71, DIO_09 73, 75, DIO_08 77, DIO_07 79, DIO_06 81, DIO_05 83, DIO_04 85, DIO_03 87, DIO_02 89, DIO_01 91, DIO_00 93, 95

BUS_WAIT# 97, BUS_BHE# 99

2 EXT_RESET#, 4 EN_USB_5V, 6 SDCARD_D2, 8 SDCARD_D3, 10 SDCARD_CMD, 12 SDCARD_3.3V, 14 SDCARD_CLK, 16 POWER, 18 SDCARD_D0, 20 SDCARD_D1

Off-Bd SD Card — uses MMC2 signals

22, 24 LCD_D00, 26 LCD_D01, 28 LCD_D02, 30 LCD_D03, 32 LCD_D04, 34 LCD_D05, 36 V_BAT, 38 LCD_D06, 40 LCD_D07, 42 LCD_D21, 44 LCD_D22, 46 LCD_D23, 48 EN_LCD_3.3V, 50, 52, 54, 56, 58, 60, 62

MUX_AD_15, MUX_AD_14, MUX_AD_13, MUX_AD_12, MUX_AD_11, MUX_AD_10, MUX_AD_09, MUX_AD_08, MUX_AD_07, MUX_AD_06, MUX_AD_05, MUX_AD_04, MUX_AD_03, MUX_AD_02, MUX_AD_01, MUX_AD_00

Data Bus or DIO

64, 66, 68, 70, 72, 74, 76, 78, 80, 82, 84, 86, 88, 90, 92, 94

96 BUS_ALE#, 98 BUS_DIR, 100 BUS_CS#

MUX_AD_[00:15]

TYCO_100PIN_SBC

Bus Control

Right

CN2

Ethernet: ETH_RX+ 1, ETH_RX- 3, ETH_CT 5, ETH_TX+ 7, ETH_TX- 9, ETH_CT 11, 3.3V 13, 15, 17, 19, 21

3.3V rail can supply up
to 700 mA to base board

NC 23, NC 25, NC 27

USB Ports: HOSTA_USB_M 29, HOSTA_USB_P 31, CPU_CORE 33, USB_OTG_M 35, USB_OTG_P 37, 3.3V 39, 41, 43, 45, 47, 49, 51, 53, 55, 57

DDR_1.5V

AVDD_OSC 59

SPI or DIO: SPI_FRM 61, SPI_MOSI 63, SPI_MISO 65, SPI_CLK 67, 69, 71, 73, 75, 77

CPU JTAG Vcc — 3.3V 79

Camera or DIO: CAM_D3 81, CAM_D4 83, CAM_PCLK 85, CAM_VCLK 87, MFP_52 89, MFP_43 91

Console: DEBUG_TXD 93, DEBUG_RXD 95

CAN: DIO_15 97, DIO_16 99

DIO_15 and DIO_16 can be CAN_TXD and CAN_RXD

2 ETH_LEFT_LED, 4 ETH_RIGHT_LED, 6 RED_LED#, 8 GREEN_LED#, 10 MFP_105, 12 MFP_106, 14 MFP_122, 16, 18, 20, 22, 24

A/D

26 MFP_49, 28 I2C_CLK, 30 I2C_DAT

I2C

32 MFP_104, 34 AUD_MCLK, 36 AUD_CLK, 38 AUD_FRM, 40 AUD_TXD, 42 AUD_RXD

I2S or DIO

44 CPU_JTAG_TMS, 46 CPU_JTAG_TCK, 48 CPU_JTAG_TDI, 50 CPU_JTAG_TDO

CPU JTAG

52 ONE_WIRE, 54 MFP_51, 56 CAM_MCLK, 58 CAM_D0, 60 CAM_D1, 62 CAM_D2, 64 CAM_D5, 66 CAM_D6, 68 CAM_D7, 70 CAM_HSYNC, 72 CAM_VSYNC

Camera or DIO

74 USB_OTG_ID, 76 USB_5V_LINE

78 UART0_TXD, 80 UART0_RXD, 82 UART1_TXD, 84 UART1_RXD, 86 UART2_TXD, 88 UART2_RXD, 90 UART3_TXD, 92 UART3_RXD, 94 UART4_TXD, 96 UART4_RXD, 98 UART5_TXD, 100 UART5_RXD

Serial Ports or DIO

TYCO_100PIN_SBC

MFP_105 and MFP_106 can be used as a second I2C bus

MFP_122 = PWM3

MFP_104 = PWM4

CN2-54 Codec CLK on the TS-8390

MFP_51, SPI_CLK, SPI_FRM, SPI_MOSI and SPI_MISO have FPGA pins in parallel

** Can use either

Boot Strap

Mode 2	TS-4700 Boots from
1	NAND Flash
0	SD Card

BUS_DIR is latched prior to OFF_BD_RESET# deasserted

Connect 1.5K ohm resistor between BUS_DIR and OFF_BD_RESET# to set low
(Boot from SD card)

BUS_DIR = MODE2

If Bus is not needed, all Bus signals can be changed to DIO

Devices connected to this bus must never drive it when BUS_CS# is deasserted
(must be off within 30 nS of deassertion)

Devices must pull the BUS_WAIT# line low if they need more than 150 nS strobe

The data bus can not have more than 30 pF of off-board capacitive loading
May need data buffer chip for heavy loads

⚠ Any I/O routed to a user accessible connector should have additional ESD protection placed on the carrier board.

Technologic Systems	Date Dec. 30, 2015
Title: TS-4700 Off-board Connectors	
Rev: C	Designer / Sheet 11 of 11