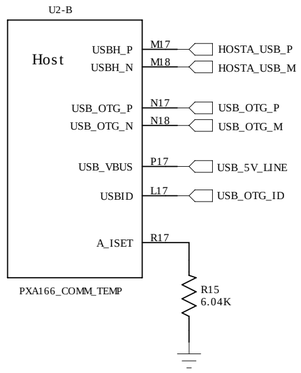
PXA166 800 MHz - PXA168 1066 MHz

USB Ports

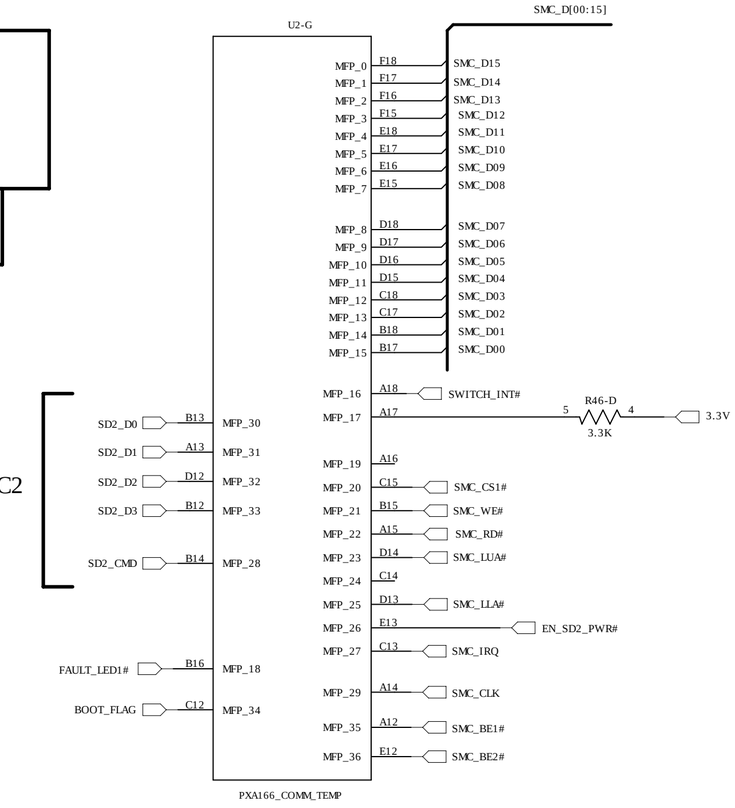


Board ID

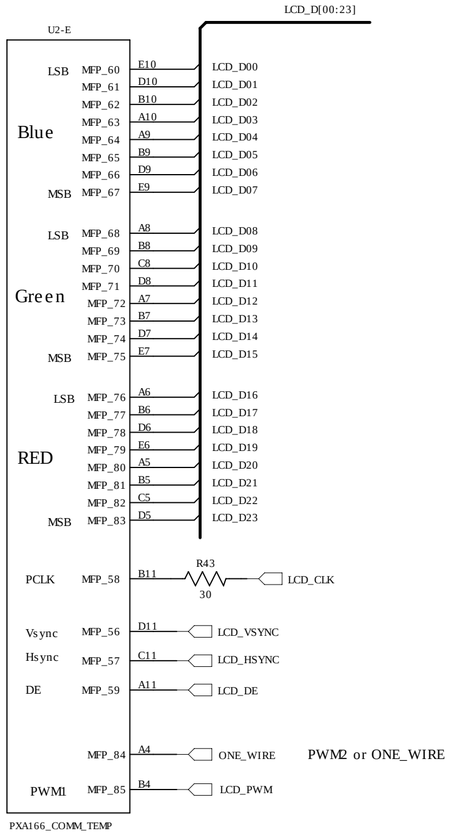
	MFP_19	MFP_17
TS-4710	1	0
TS-4712	1	1
TS-4720	0	1

Requires MFP to be Inputs
and weak PU turned ON

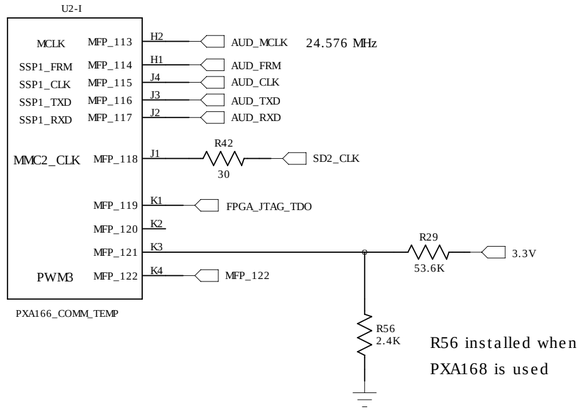
SMC Bus



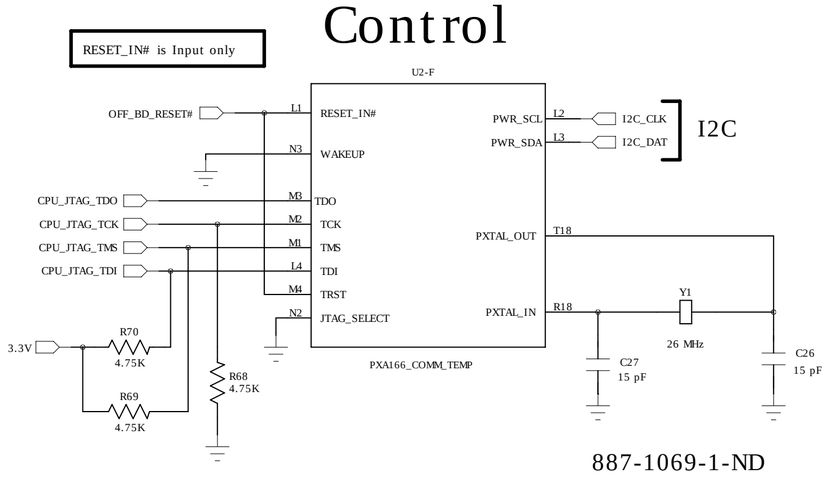
LCD



I2S

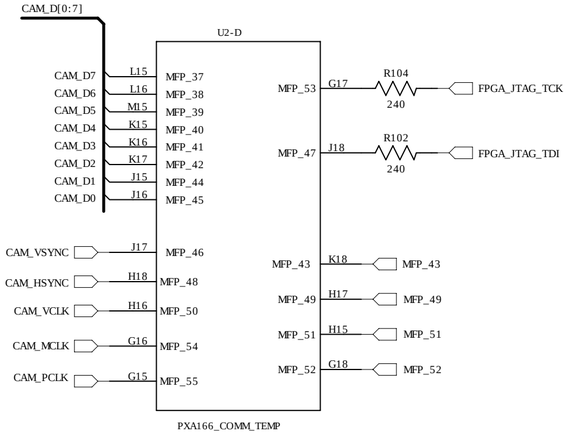


Control



887-1069-1-ND

Camera

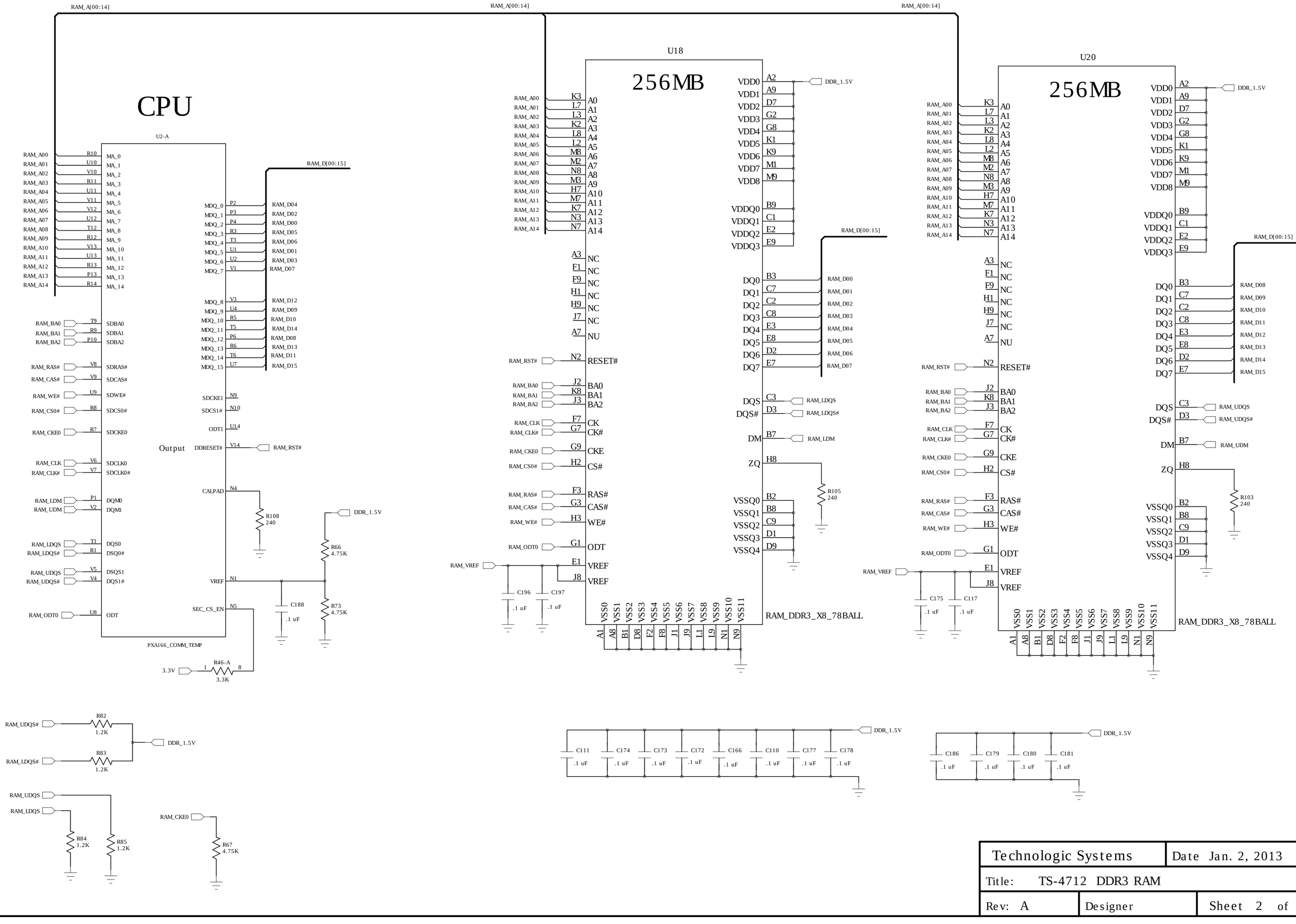


Technologic Systems	Date Jan. 2, 2013	
Title: TS-4712 Marvell PXA166 or PXA168		
Rev: A	Designer	Sheet 1 of 10

DDR3 x8 RAM

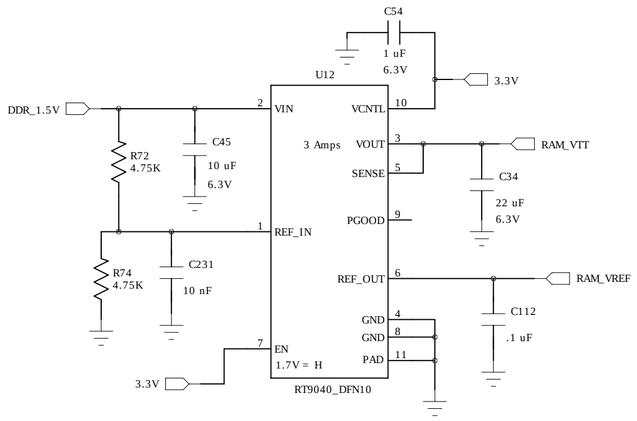
2 Gbit RAM chips

512 MB RAM Total

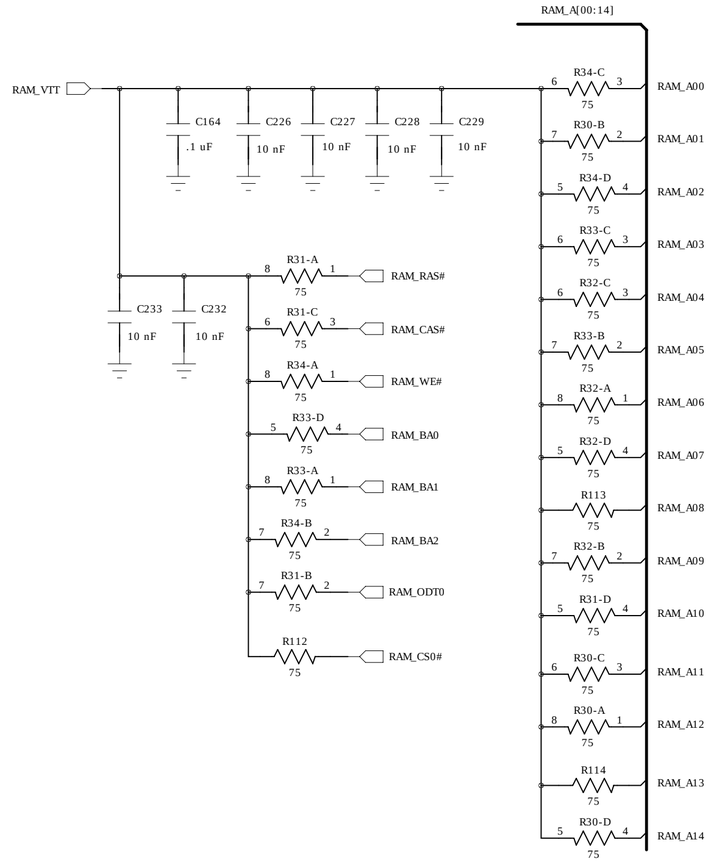


Technologic Systems		Date Jan. 2, 2013
Title: TS-4712 DDR3 RAM		
Rev: A	Designer	Sheet 2 of 10

DDR3 RAM Termination Power Supply



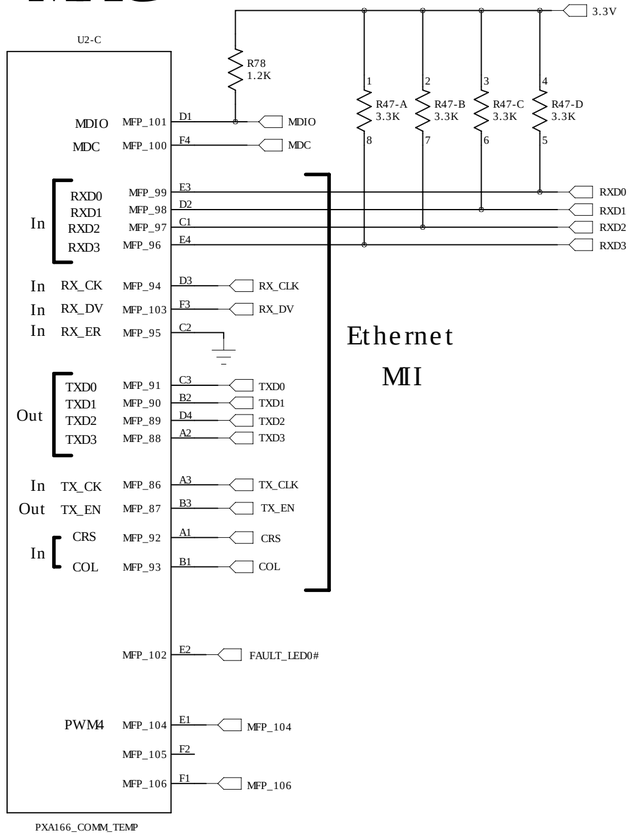
Termination Resistors



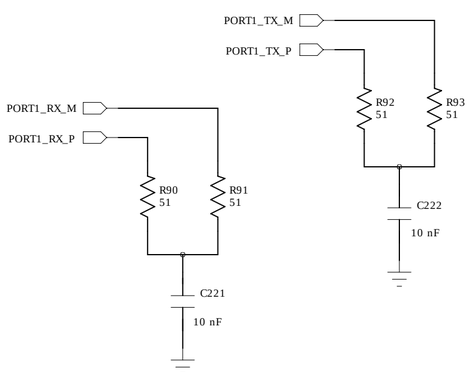
Technologic Systems	Date Jan. 2, 2013	
Title: TS-4712 DDR3 RAM		
Rev: A	Designer	Sheet 3 of 10

10/100 Ethernet 4-Port Switch

CPU MAC

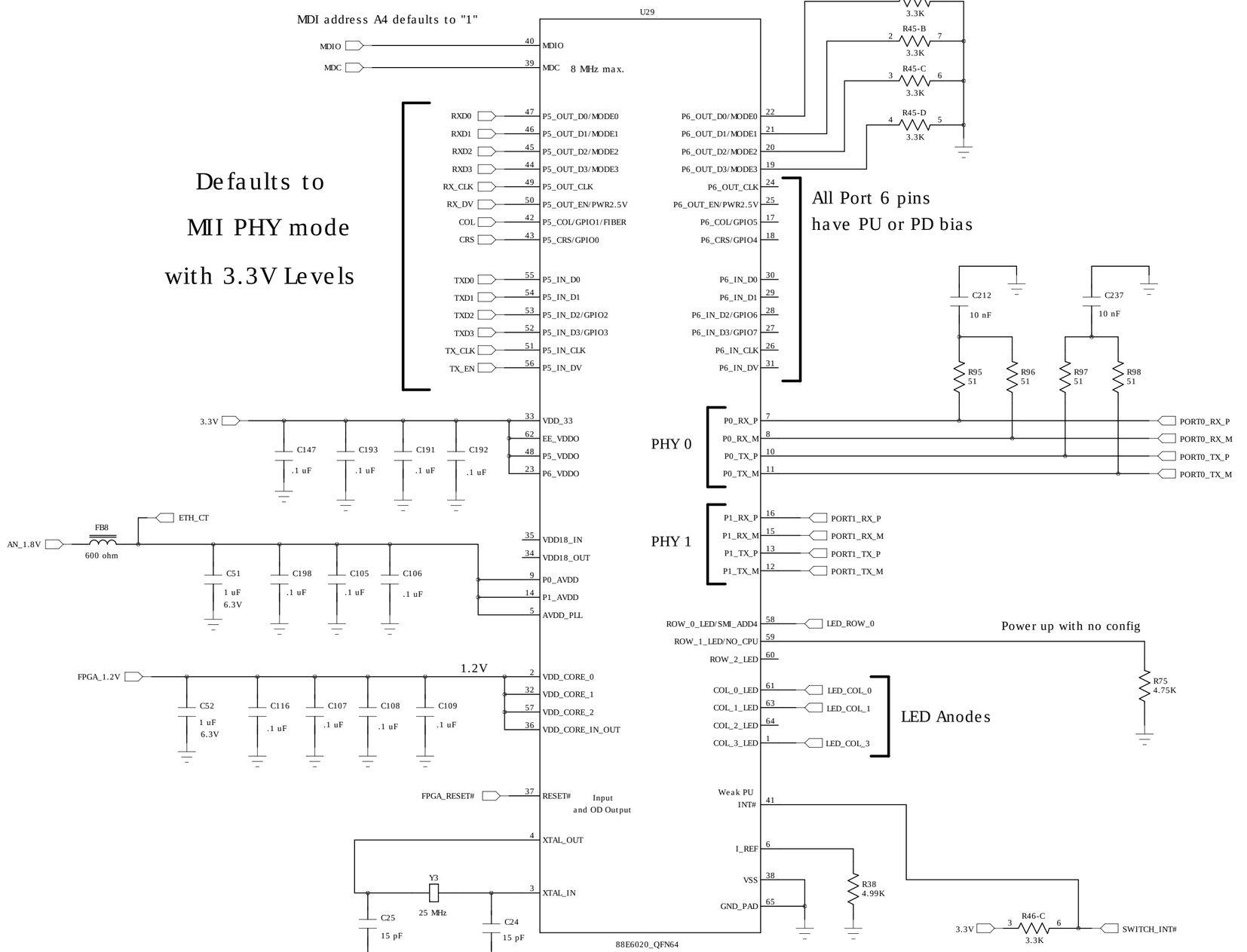


Ethernet MII



MDI address A4 defaults to "1"

Defaults to MII PHY mode with 3.3V Levels

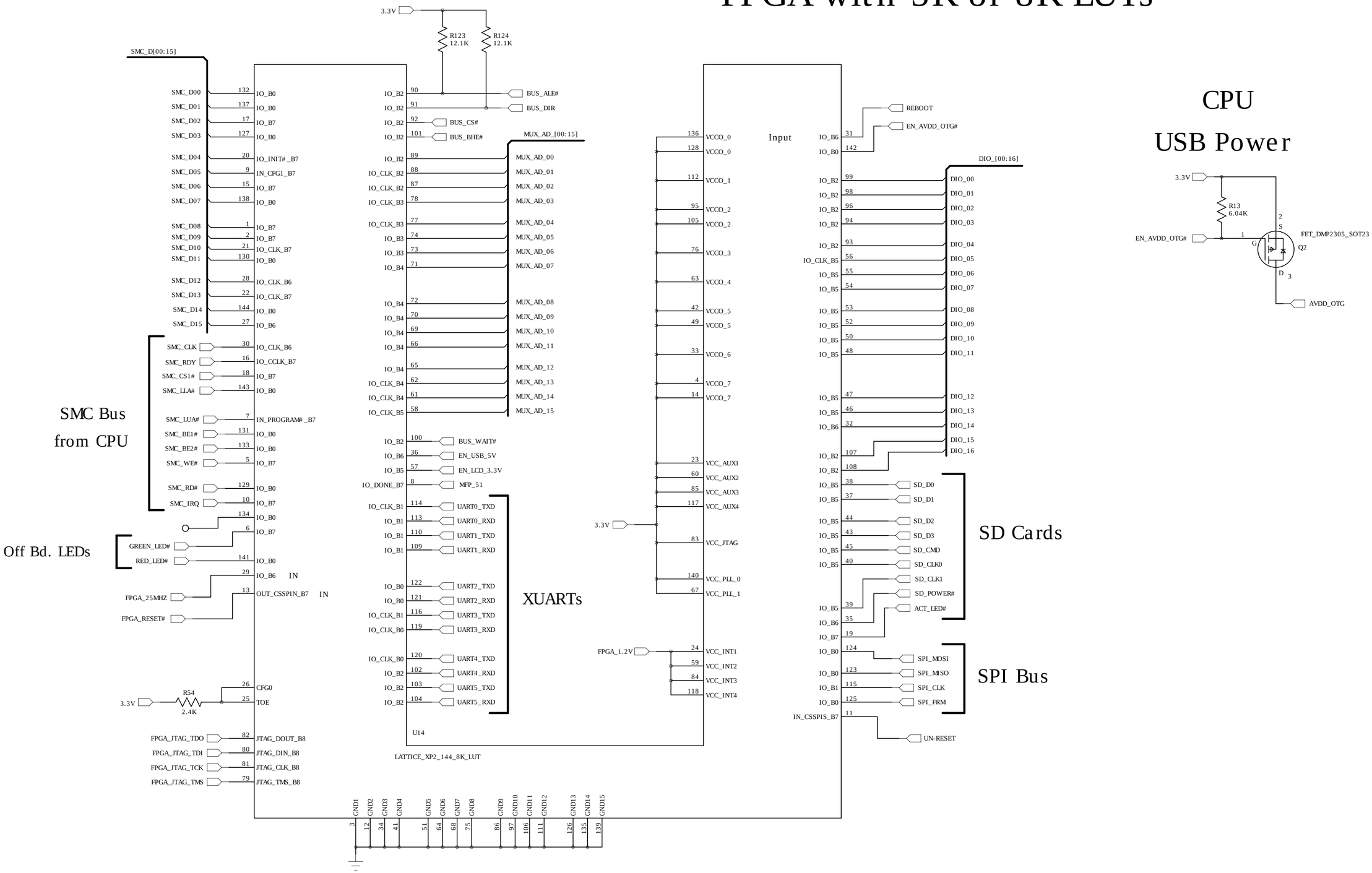


Auto MDIX is supported

Polarity Correction also supported

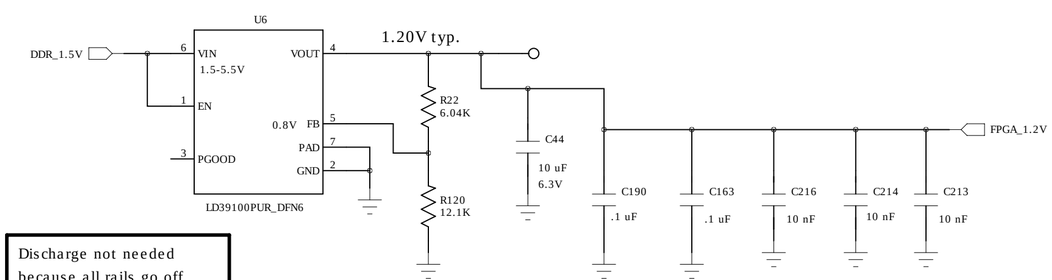
Technologic Systems		Date Jan. 2, 2013
Title: TS-4712 Ethernet Switch		
Rev: A	Designer RLM	Sheet 4 of 10

FPGA with 5K or 8K LUTs



CPU USB Power

FPGA 1.2V Reg.



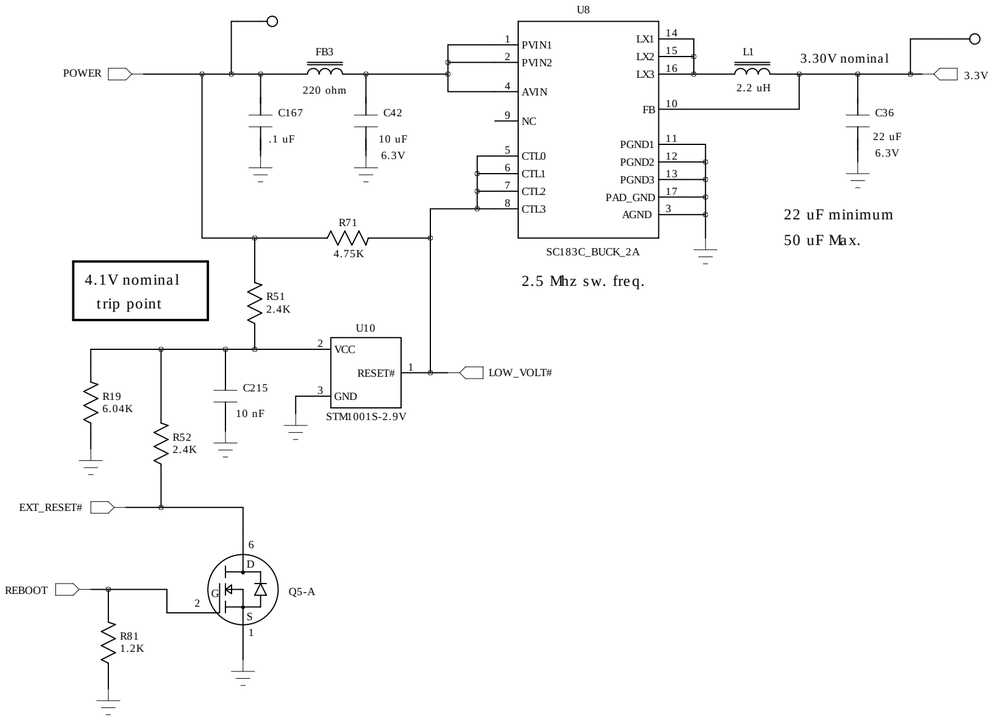
Discharge not needed because all rails go off for 200 mS

Technologic Systems	Date Jan. 2, 2013	
Title: TS-4712 FPGA		
Rev: A	Designer	Sheet 5 of 10

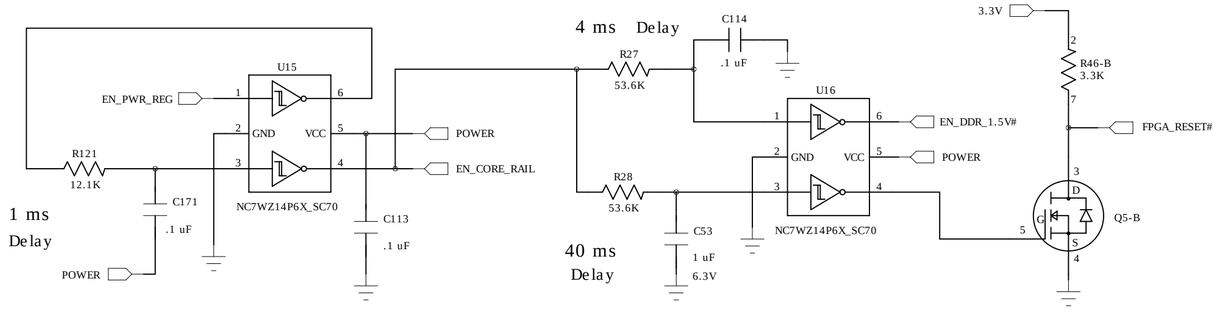
Power Supplies

#1 3.3V Power Supply

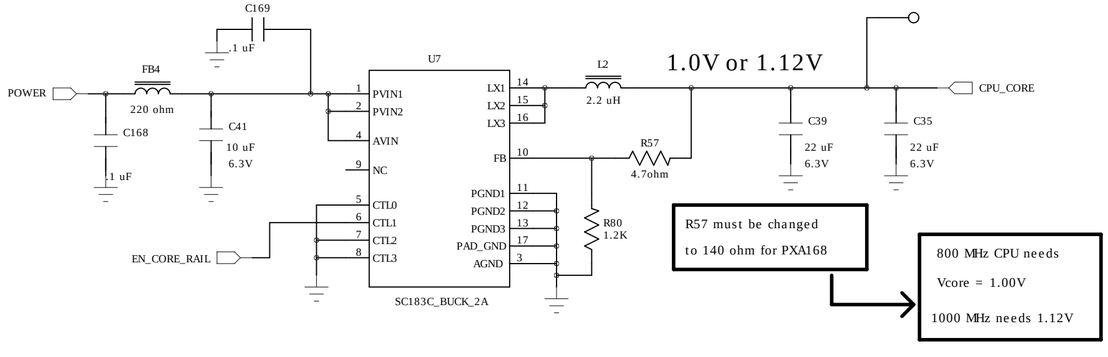
up to 2000 mA



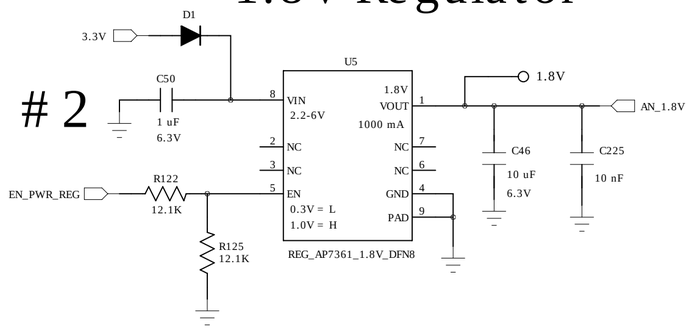
Power Sequencer



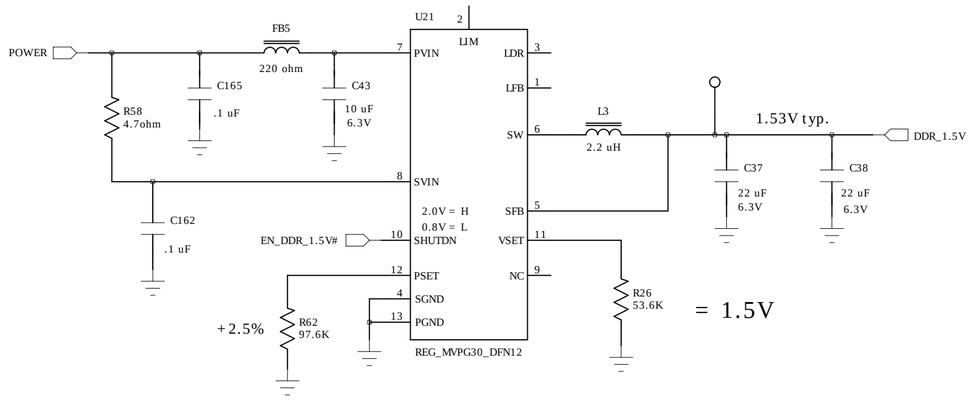
#3 CPU Core Supply



Analog 1.8V Regulator

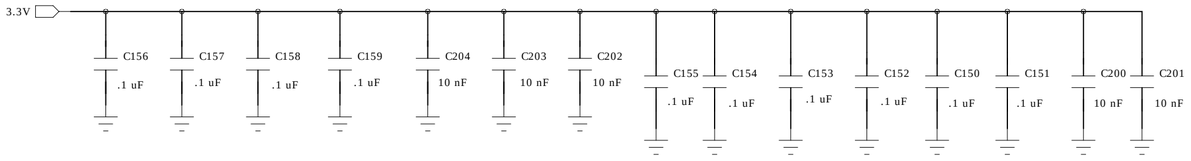


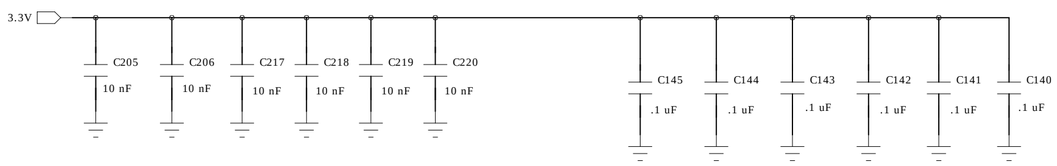
#4 DDR3 1.5V Reg.

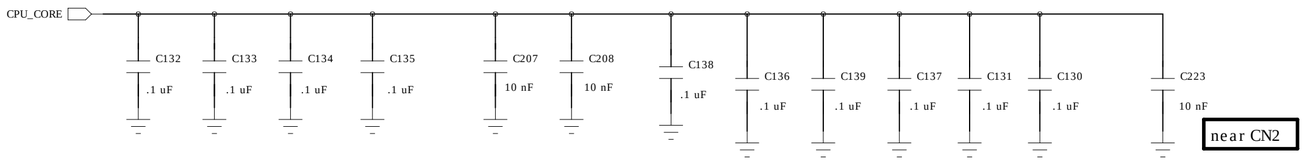


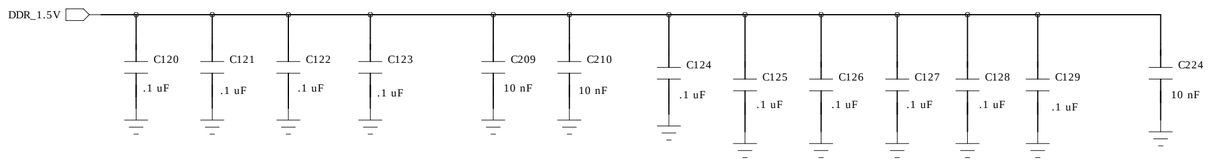
Technologic Systems	Date Jan. 2, 2013	
Title: TS-4712 Power Supplies		
Rev: A	Designer	Sheet 6 of 10

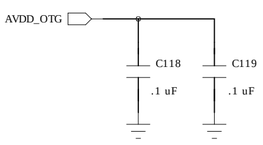
CPU Power





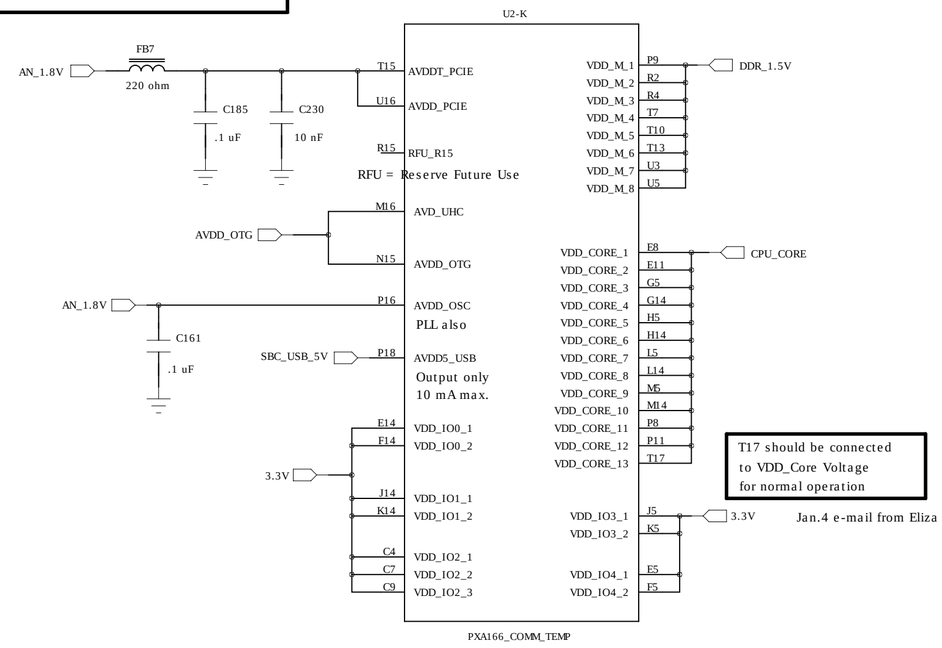




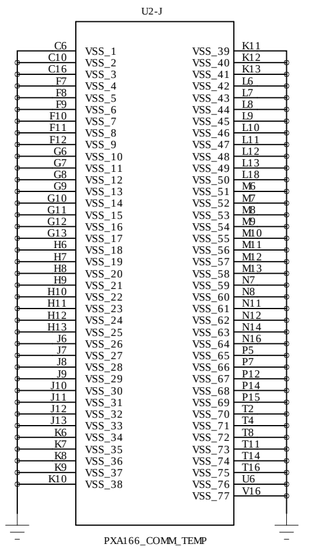


PXA168 PCIE rails must be connected to AN_1.8V

CPU

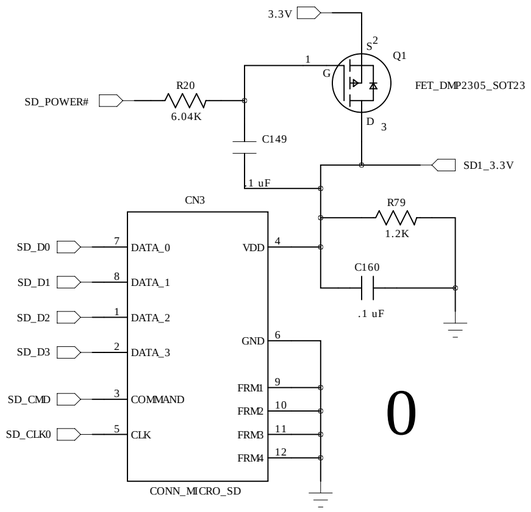


CPU

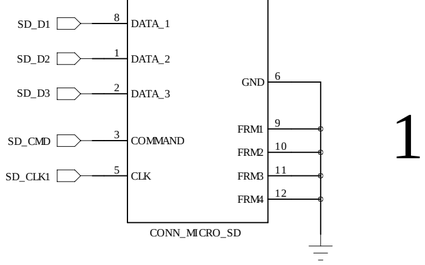


Technologic Systems		Date Jan. 2, 2013
Title: TS-4712 CPU Power and Bypass caps		
Rev: A	Designer	Sheet 7 of 10

Micro SD Card Sockets

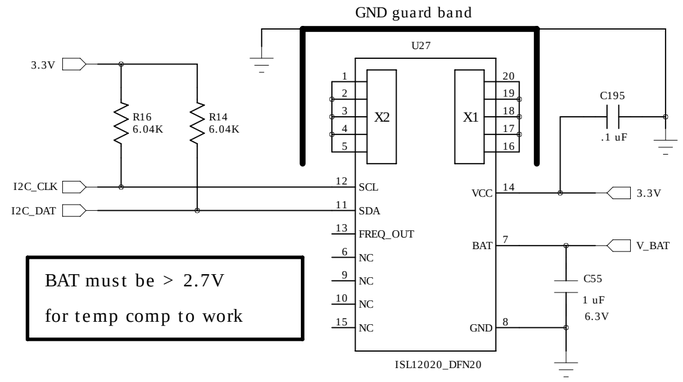


0



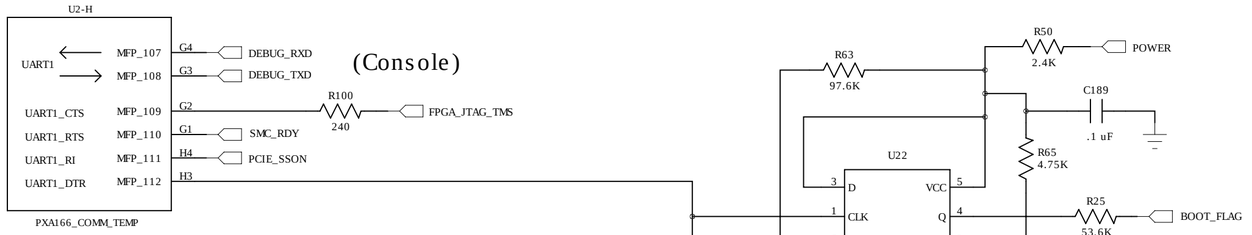
1

RTC and Temp. Sensor



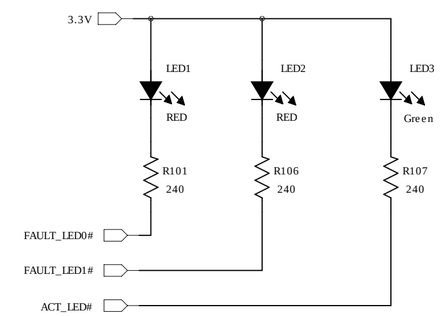
BAT must be > 2.7V
for temp comp to work

CPU Debug UART

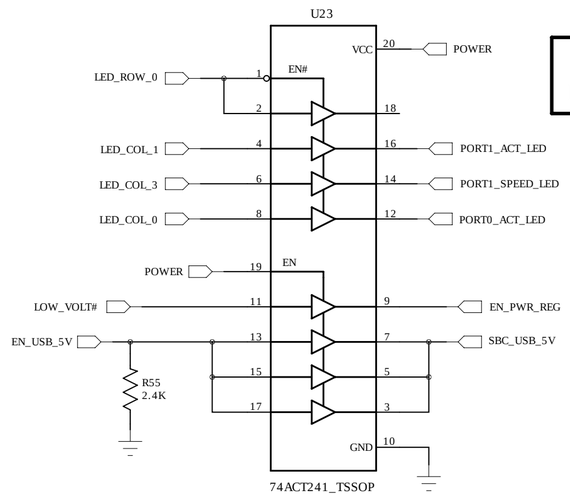


Reboot Flag

SD Card LEDs

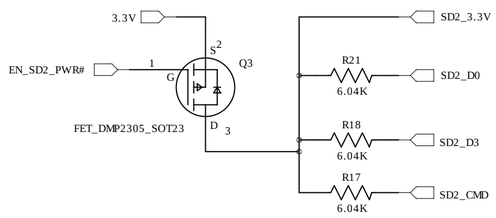


3.3V --> 5V Level Shifter



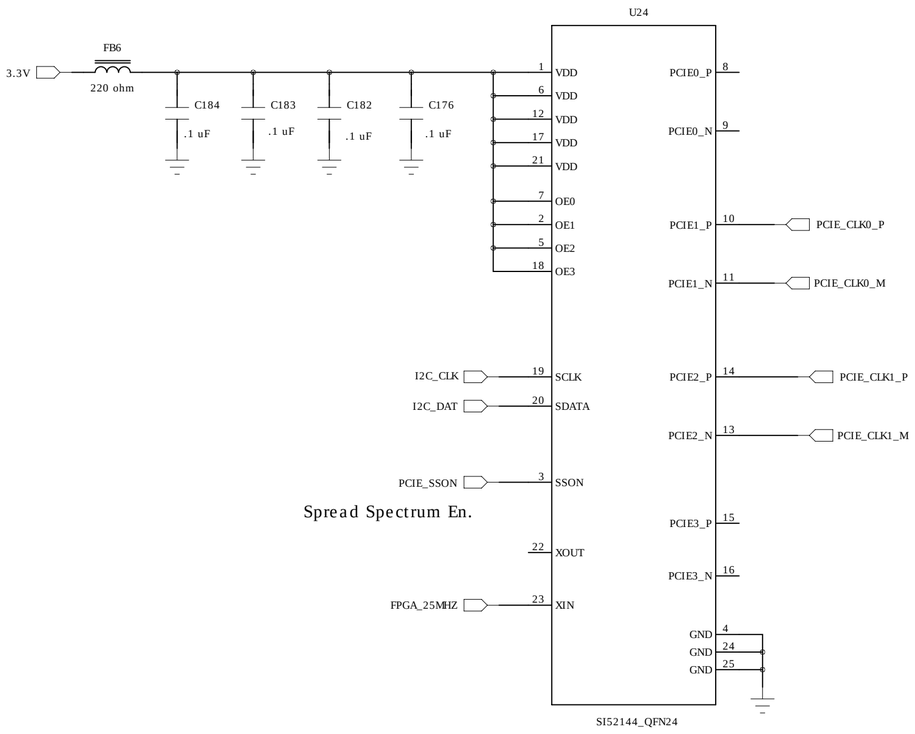
Off-Board LEDs
have cathode to GND

OFF BD. SD Card Power



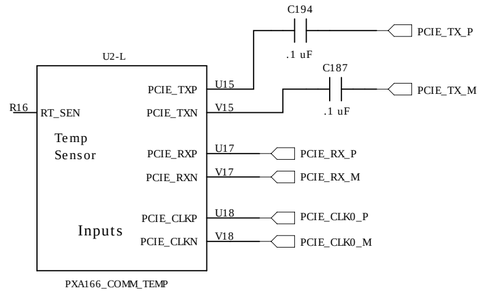
Technologic Systems	Date Jan. 2, 2013	
Title: TS-4712 SD card, RTC, Temp.		
Rev: A	Designer	Sheet 8 of 10

PCIe 100 MHz Clock Generator



CPU PCIe

PCIe not supported on PXA166



PXA166 and PXA168 BOM Differences

R57 = 140 ohm for PXA168

R56 removed for PXA166

FB6, FB7 removed for PXA166

U24 removed for PXA166

U2 = PXA166 Commercial Temp

or = PXA168 Industrial Temp

Technologic Systems		Date Jan. 2, 2013
Title: TS-4712 PCIe Clock and CPU PCIe		
Rev: A	Designer	Sheet 9 of 10

Two 100-pin Off-board Connectors

"POWER" pins supply all power to the module
Apply 4.5V to 5.5V to these pins

Current drain is approximately 400 mA

EXT_RESET# is an Input
used to reboot the CPU

Do not drive active high
(use open drain)

⚠ All signals driving DIO on CN1 & CN2 must be powered by the 3.3V on CN2, or remain at 0V until the CN2 3.3V rail is > 3.0V

Must have 10 nF Capacitor
very near CN2 and GND
for all "quiet" signals
(between diff pairs)

⚠ Pin 1 is the top left corner pin on the connector. All of the pins on the left are odd numbered. This may differ from the connector manufacture's datasheet.

Left

CN1

FPGA JTAG: FPGA_JTAG_TMS (1), FPGA_JTAG_TCK (3), FPGA_JTAG_TDO (5), FPGA_JTAG_TDI (7), OFF_BD_RESET# (9)

OFF_BD_RESET# is an Output
used to reset all peripherals

NC (11), NC (13), POWER (15), POWER_FAIL# NC (17)

LCD_D08 (19), LCD_D09 (21), LCD_D10 (23), LCD_D11 (25), LCD_D12 (27), 29

POWER — C146 .1 uF, C148 .1 uF

LCD_D13 (31), LCD_D14 (33), LCD_D15 (35), LCD_D16 (37), LCD_D17 (39), LCD_D18 (41), LCD_D19 (43), LCD_D20 (45), POWER (47)

LCD_CLK (49), LCD_HSYNC (51), LCD_VSYNC (53), LCD_DE (55), LCD_PWM (57), 59

DIO_[00:16] (61)

FPGA DIO: DIO_14 (63), DIO_13 (65), DIO_12 (67), DIO_11 (69), DIO_10 (71), DIO_09 (73), 75, DIO_08 (77), DIO_07 (79), DIO_06 (81), DIO_05 (83), DIO_04 (85), DIO_03 (87), DIO_02 (89), DIO_01 (91), DIO_00 (93), 95

BUS_WAIT# (97), BUS_BHE# (99)

2 EXT_RESET#, 4 EN_USB_5V, 6 SD2_D2, 8 SD2_D3, 10 SD2_CMD, 12 SD2_3.3V, 14 SD2_CLK, 16 POWER, 18 SD2_D0, 20 SD2_D1

Off-Bd SD Card
uses CPU MMC2

22, 24 LCD_D00, 26 LCD_D01, 28 LCD_D02, 30 LCD_D03, 32 LCD_D04, 34 LCD_D05, 36 V_BAT, 38 LCD_D06, 40 LCD_D07, 42 LCD_D21, 44 LCD_D22, 46 LCD_D23, 48 EN_LCD_3.3V, 50, 52, 54, 56, 58, 60, 62

Data Bus or DIO: 64 MUX_AD_15, 66 MUX_AD_14, 68 MUX_AD_13, 70 MUX_AD_12, 72 MUX_AD_11, 74 MUX_AD_10, 76 MUX_AD_09, 78 MUX_AD_08, 80 MUX_AD_07, 82 MUX_AD_06, 84 MUX_AD_05, 86 MUX_AD_04, 88 MUX_AD_03, 90 MUX_AD_02, 92 MUX_AD_01, 94 MUX_AD_00

96 BUS_ALE#, 98 BUS_DIR, 100 BUS_CS#

MUX_AD_[00:15]

TYCO_100PIN_MODULE

Bus Control

If Bus is not needed, all Bus signals can be changed to DIO

⚠ Any I/O routed to a user accessible connector should have additional ESD protection placed on the carrier board.

Devices connected to this bus must never drive it when BUS_CS# is deasserted
(must be off within 30 nS of deassertion)

Devices must pull the BUS_WAIT# line low if they need more than 150 nS strobe

The data bus can not have more than 30 pF of off-board capacitive loading
May need data buffer chip for heavy loads

Right

CN2

Primary Ethernet: PORT1_RX_P (1), PORT1_RX_M (3), ETH_CT (5), PORT1_TX_P (7), PORT1_TX_M (9), ETH_CT (11), 3.3V (13), 15, 17, 19, 21

3.3V rail can supply up to 700 mA to base board

NC (23), NC (25), NC (27), 29

Maximum off-board load on AN_1.8V is 10 mA

USB Ports: HOSTA_USB_M (31), HOSTA_USB_P (33), CPU_CORE (35), USB_OTG_M (37), USB_OTG_P (39)

3.3V — C235 10 nF

41, 43, 45

PCIE_TX_M (47), PCIE_TX_P (49), 51

PCIE_RX_M (53), PCIE_RX_P (55), 57

DDR_1.5V — C234 10 nF

PCIE_CLK1_M (59), PCIE_CLK1_P (61), AN_1.8V (63)

SPI or DIO: SPI_FRM (65), SPI_MOSI (67), SPI_MISO (69), SPI_CLK (71), 73

CPU JTAG Vcc — 3.3V — 75, 77, 79

Max. load on JTAG_Vcc (CN2-79) is 20 mA
Not always 3.3V

Camera or DIO: CAM_D3 (81), CAM_D4 (83), CAM_PCLK (85), CAM_VCLK (87), MFP_52 (89), MFP_43 (91)

Console: DEBUG_TXD (93), DEBUG_RXD (95)

CAN: DIO_15 (97), DIO_16 (99)

DIO_15 and DIO_16 can be CAN_TXD and CAN_RXD

2 PORT1_ACT_LED, 4 PORT1_SPEED_LED, 6 RED_LED#, 8 GREEN_LED#, 10 PORT0_ACT_LED, 12 MFP_106, 14 MFP_122

MFP_122 = PWM3

2nd Ethernet Port: 16 PORT0_RX_P, 18 PORT0_RX_M, 20 ETH_CT, 22 PORT0_TX_P, 24 PORT0_TX_M

26 MFP_49, I2C: 28 I2C_CLK, 30 I2C_DAT

32 MFP_104

MFP_104 = PWM4

I2S or DIO: 34 AUD_MCLK, 36 AUD_CLK, 38 AUD_FRM, 40 AUD_TXD, 42 AUD_RXD

CPU JTAG: 44 CPU_JTAG_TMS, 46 CPU_JTAG_TCK, 48 CPU_JTAG_TDI, 50 CPU_JTAG_TDO

52 ONE_WIRE, 54 MFP_51

CN2-54 Codec CLK on the TS-8390

MFP_51 has FPGA pin in parallel
** Can use either

Camera or DIO: 56 CAM_MCLK, 58 CAM_D0, 60 CAM_D1, 62 CAM_D2, 64 CAM_D5, 66 CAM_D6, 68 CAM_D7, 70 CAM_HSYNC, 72 CAM_VSYNC

74 USB_OTG_ID, 76 USB_5V_LINE

Serial Ports or DIO: 78 UART0_TXD, 80 UART0_RXD, 82 UART1_TXD, 84 UART1_RXD, 86 UART2_TXD, 88 UART2_RXD, 90 UART3_TXD, 92 UART3_RXD, 94 UART4_TXD, 96 UART4_RXD, 98 UART5_TXD, 100 UART5_RXD

TYCO_100PIN_MODULE

ETH_CT — C115 .1 uF, C238 10 nF — near CN2-20

Technologic Systems	Date Jan. 2, 2013	
Title: TS-4712 Off-board Connectors		
Rev: A	Designer	Sheet 10 of 10