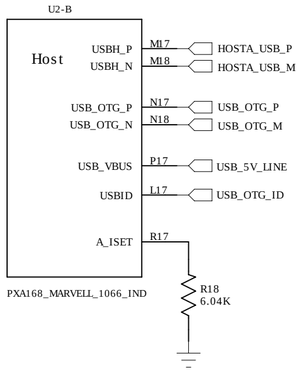
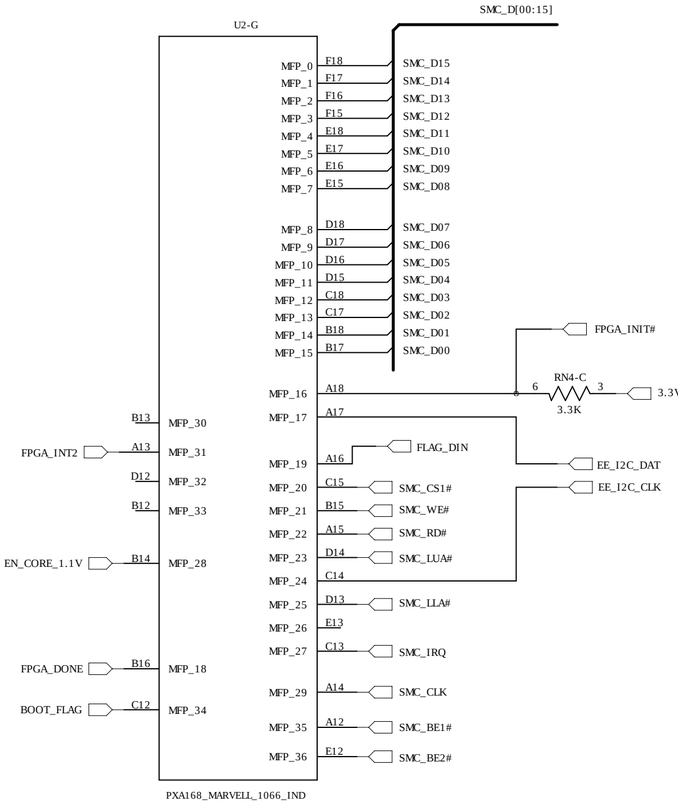
PXA168 1066 MHz

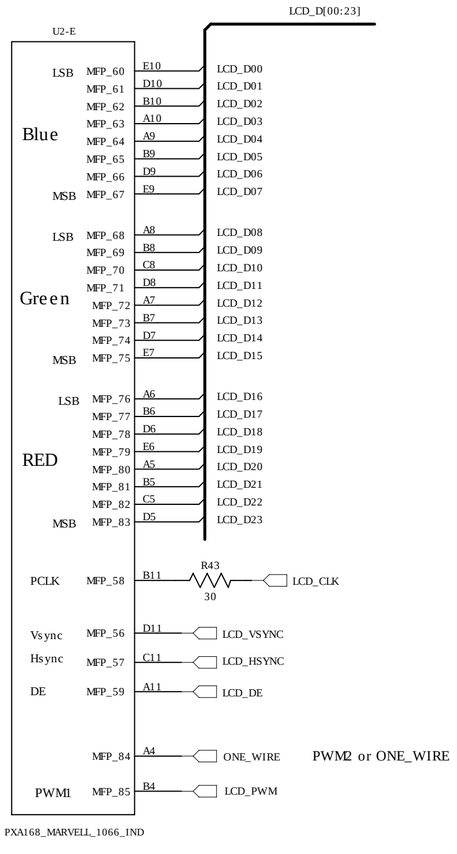
USB Ports



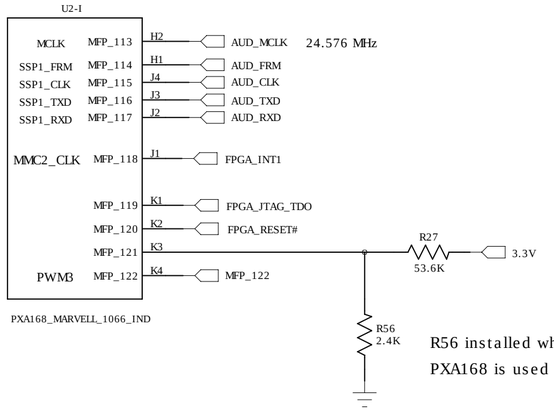
SMC Bus



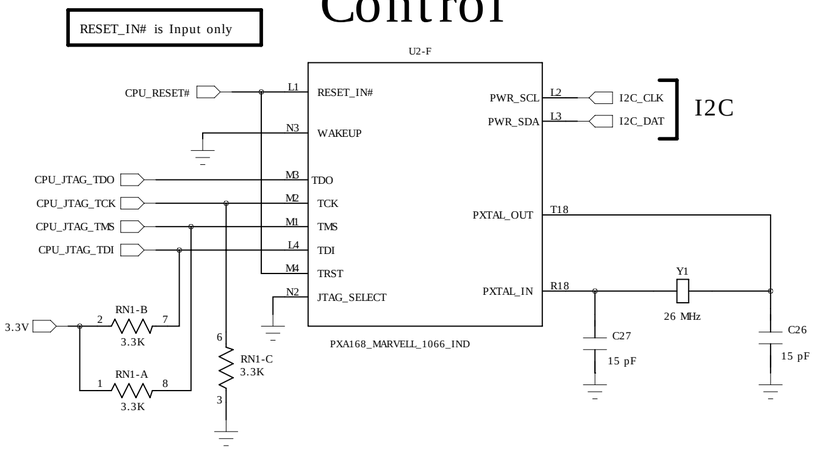
LCD



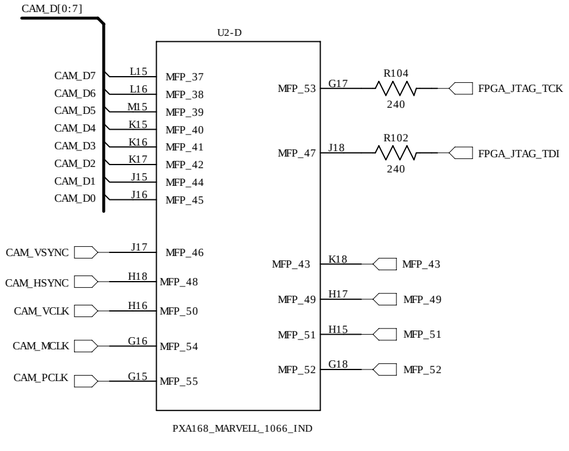
I2S



Control



Camera

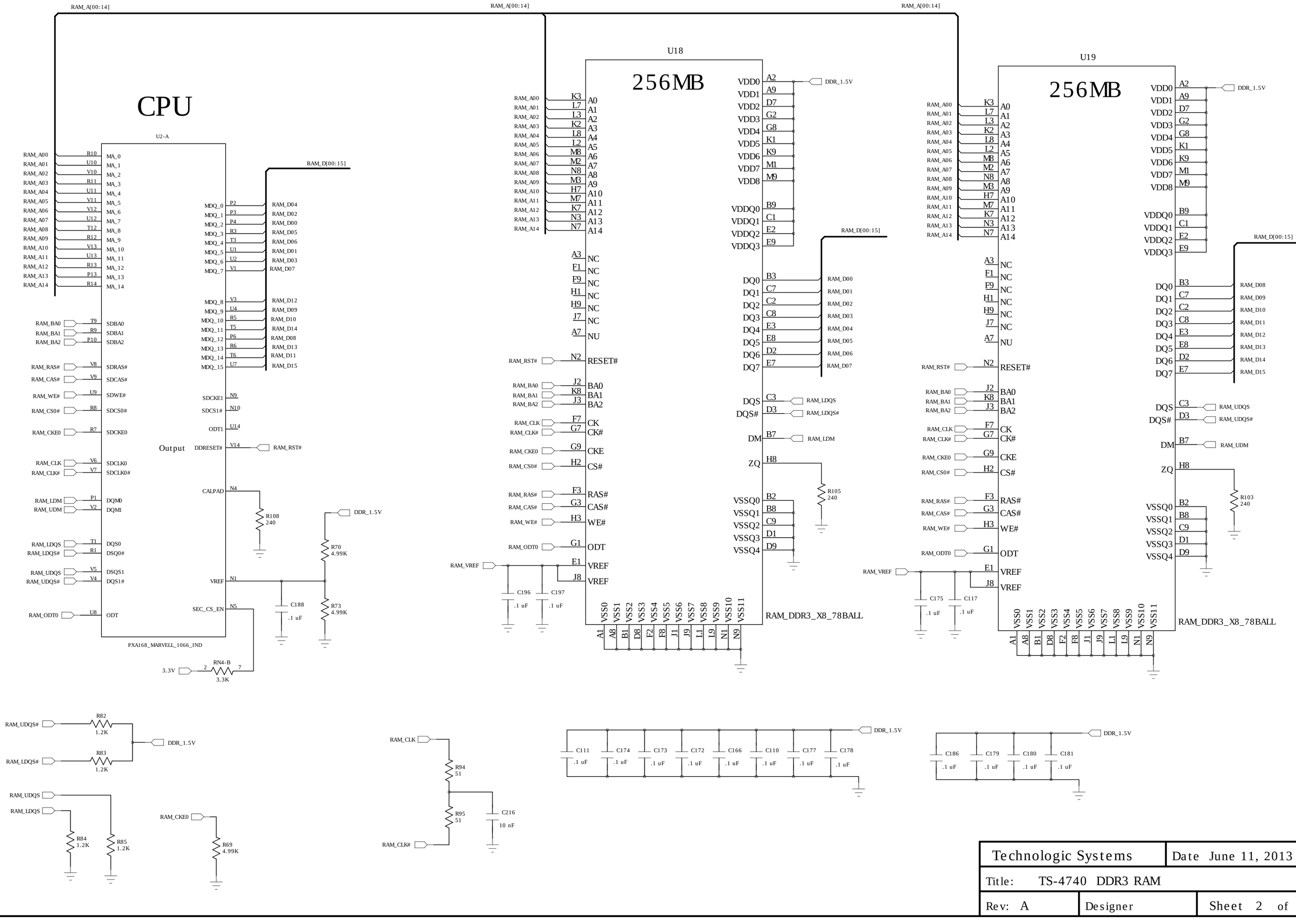


Technologic Systems		Date June 11, 2013
Title: TS-4740 Marvell PXA168		
Rev: A	Designer	Sheet 1 of 13

DDR3 x8 RAM

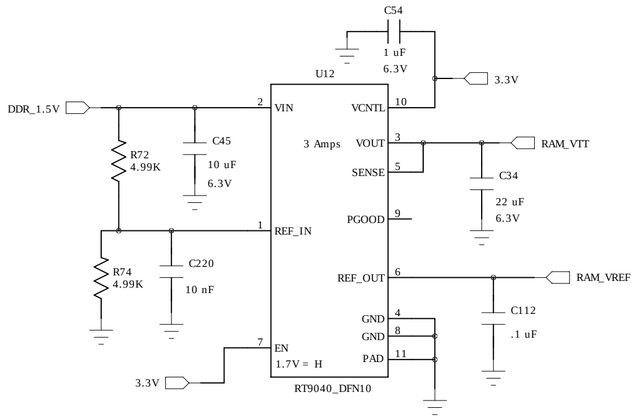
2 Gbit RAM chips

512 MB RAM Total

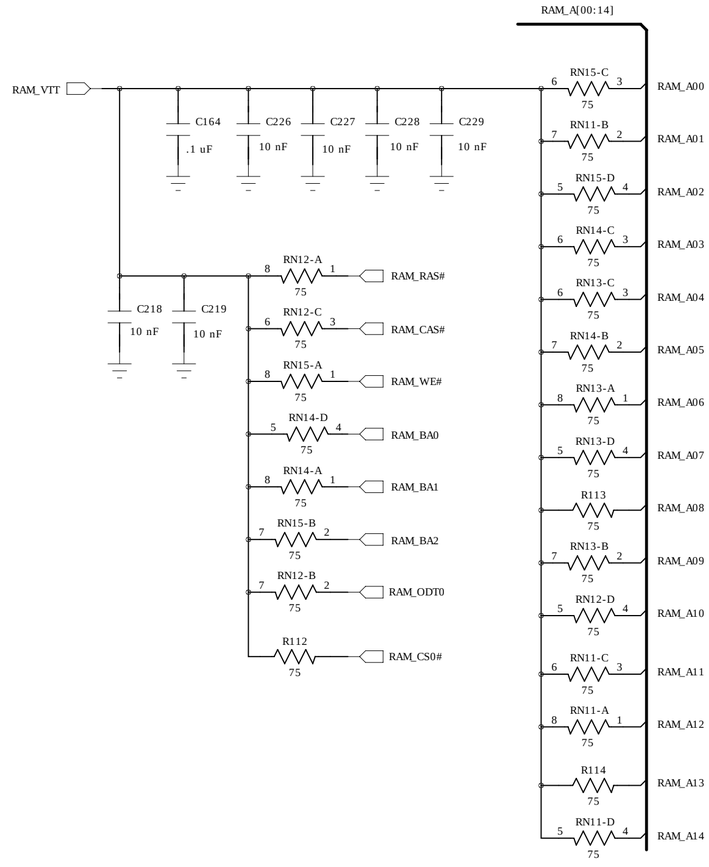


Technologic Systems		Date June 11, 2013
Title: TS-4740 DDR3 RAM		
Rev: A	Designer	Sheet 2 of 13

DDR3 RAM Termination Power Supply



Termination Resistors



Technologic Systems		Date June 11, 2013
Title: TS-4740 DDR3 RAM		
Rev: A	Designer	Sheet 3 of 13

10/100 Ethernet Port

CPU

MAC

U2-C

	MDIO	MFP_101	D1
	MDC	MFP_100	F4
In	RXD0	MFP_99	E3
In	RXD1	MFP_98	D2
In	RXD2	MFP_97	C1
In	RXD3	MFP_96	E4
In	RX_CK	MFP_94	D3
In	RX_DV	MFP_103	F3
In	RX_ER	MFP_95	C2
Out	TXD0	MFP_91	C3
Out	TXD1	MFP_90	B2
Out	TXD2	MFP_89	D4
Out	TXD3	MFP_88	A2
In	TX_CK	MFP_86	A3
Out	TX_EN	MFP_87	B3
In	CRS	MFP_92	A1
In	COL	MFP_93	B1
		MFP_102	E2
	PWM4	MFP_104	E1
		MFP_105	F2
		MFP_106	F1

PXA168_MARVELL_1066_IND

3.3V

R80 1.2K

R68 4.99K

R75 4.99K

FPGA_RESET#

MFP_104

MFP_106

U13

16	MDIO		
17	MDC		
11	RXD0/MDE0		
10	RXD1/MODE1		
9	RXD2/RMIISEL		
8	RXD3/PHYAD2		
7	RXCLK/PHYAD1		
26	RXDV		
13	RXER/RXD4/PHYAD0		
22	TXD0		
23	TXD1		
24	TXD2		
25	TXD3		
20	TXCLK		
21	TXEN		
14	CRS		
15	COL/CRS_DV/MODE2		
18	INT/TXER/TXD4		
19	RESET#		VDD_IO max
4	XTAL2		
	VDD_2A		
5	XTAL1/CLKIN		
32	RBIAS		
		27	VDD_1A
		1	VDD_2A
		12	VDD_IO
		6	VDD_CR
		31	RXP
		30	RXN
		29	TXP
		28	TXN
	LED1/REGOFF	3	
	VDD_2A		
	LED2/INTSEL	2	
	VSS	33	

FPGA_25MHZ

R130 12.1K

R20 6.04K

R119 12.1K

LAN8710i

FB1 220 ohm

FB8 600 ohm

3.3V

C140 .1 uF

C193 .1 uF

C56 1 uF 6.3V

C51 1 uF 6.3V

C143 .1 uF

C205 10 nF

C52 1 uF 6.3V

C214 10 nF

R90 51

R91 51

R60 4.7ohm

C142 .1 uF

C212 10 nF

FE_CT

FE_RX_P

FE_RX_M

R92 51

R93 51

C116 .1 uF

FE_TX_P

FE_TX_M

FE_ACT_LED

LAN8710 can power sequence in any order

Internal 1.2V Reg. can be turned off by having LED1 high

Using Sw. 1.2V Reg. saves 13 mA @ 5V

Total chip power: 160mw --> 100 mw

1.2V Core

near CN2

Must have no aggressor signals near 12.1K resistor Trace short as possible

PHY address = 0

MDIO bus can not be used until 100 uS after Reset# is deasserted

MDCLK max is 2.5 MHz

PHY address and modes latched on rising edge of Reset#

Put MX515 in MII mode before deasserting Reset#

LED high voltage is VDD_2A = 3.3V

LED1 = Activity/Link

LED2 = Speed 100 Mbit

Technologic Systems	Date June 11, 2013	
Title: TS-4740 10/100 Ethernet PHY		
Rev: A	Designer RLM	Sheet 4 of 13

Xilinx LX25T_324 FPGA

25K equivalent LUTs
(15K 6-input LUTs)

177 DIO

30K Flip-flops

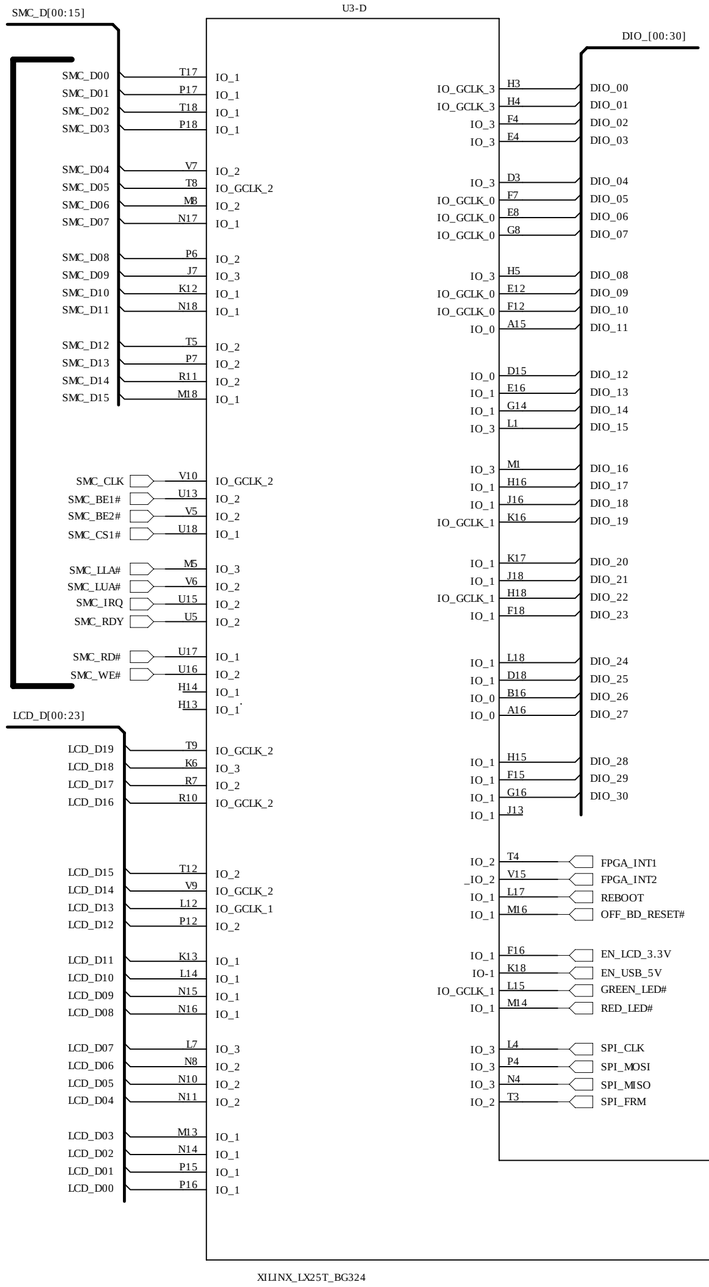
52 [2K x 9] Block RAM

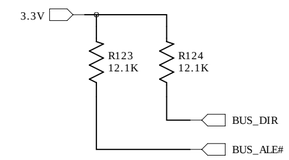
2 PLLs + 4 DCMs

38 18x18 Multipliers

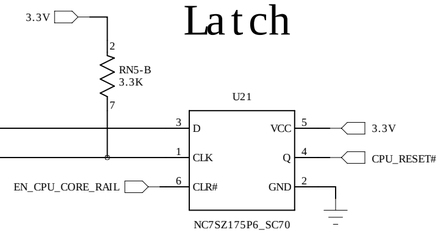
Each Mult. has an adder and accumulator

Interface to CPU





CPU Reset Latch



Bit stream should initialize
EN_AVDD_OTG# deasserted (high)

After FPGA_RESET# deasserted,
It should assert EN_AVDD_OTG#

Then wait 10 ms, and write
a "1" into the CPU RESET Latch

Power up

FPGA_RESET# will still be asserted
after FPGA is configured
and can be used as a FPGA reset

CPU reload bit stream

CPU can also drive FPGA_RESET#
low during a "soft" FPGA update

REBOOT = "Cold Boot" causes
LOW_VOLT# to be asserted
This will collapse all rails and
it will assert CPU reset and
will reload FPGA from Flash

This will clear Boot Flag

"Warm Reboot" occurs
by clearing Reset Latch
This will reload the FPGA

This will not clear Boot Flag

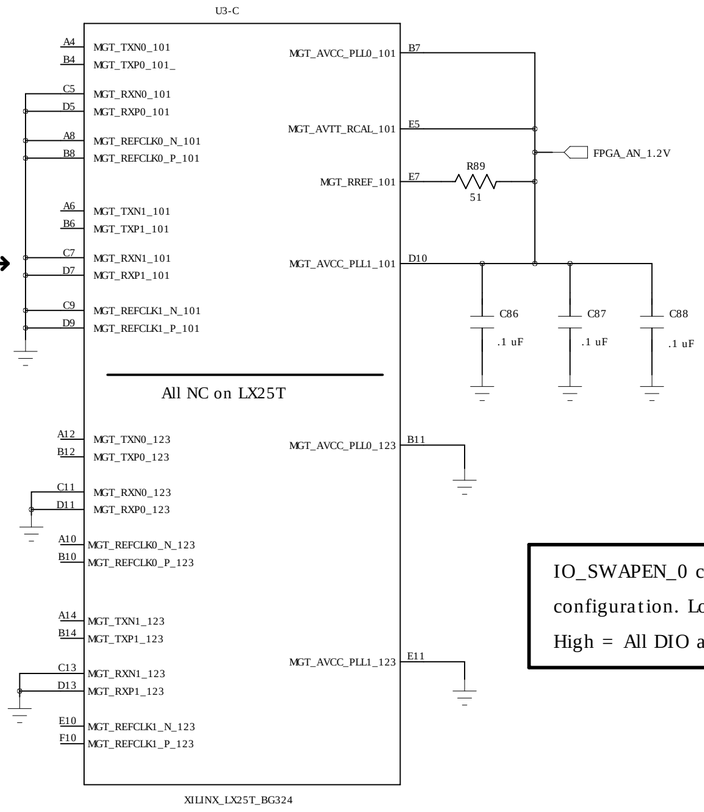
Technologic Systems	Date June 11, 2013	
Title: TS-4740 Xilinx FPGA		
Rev: A	Designer	Sheet 5 of 13

Xilinx LX25T_324 FPGA

Gigabit Transceivers

Page 162 GTP User Guide

Page 168-169
REF_CLK Inputs have internal 100 ohm term. must be cap coupled

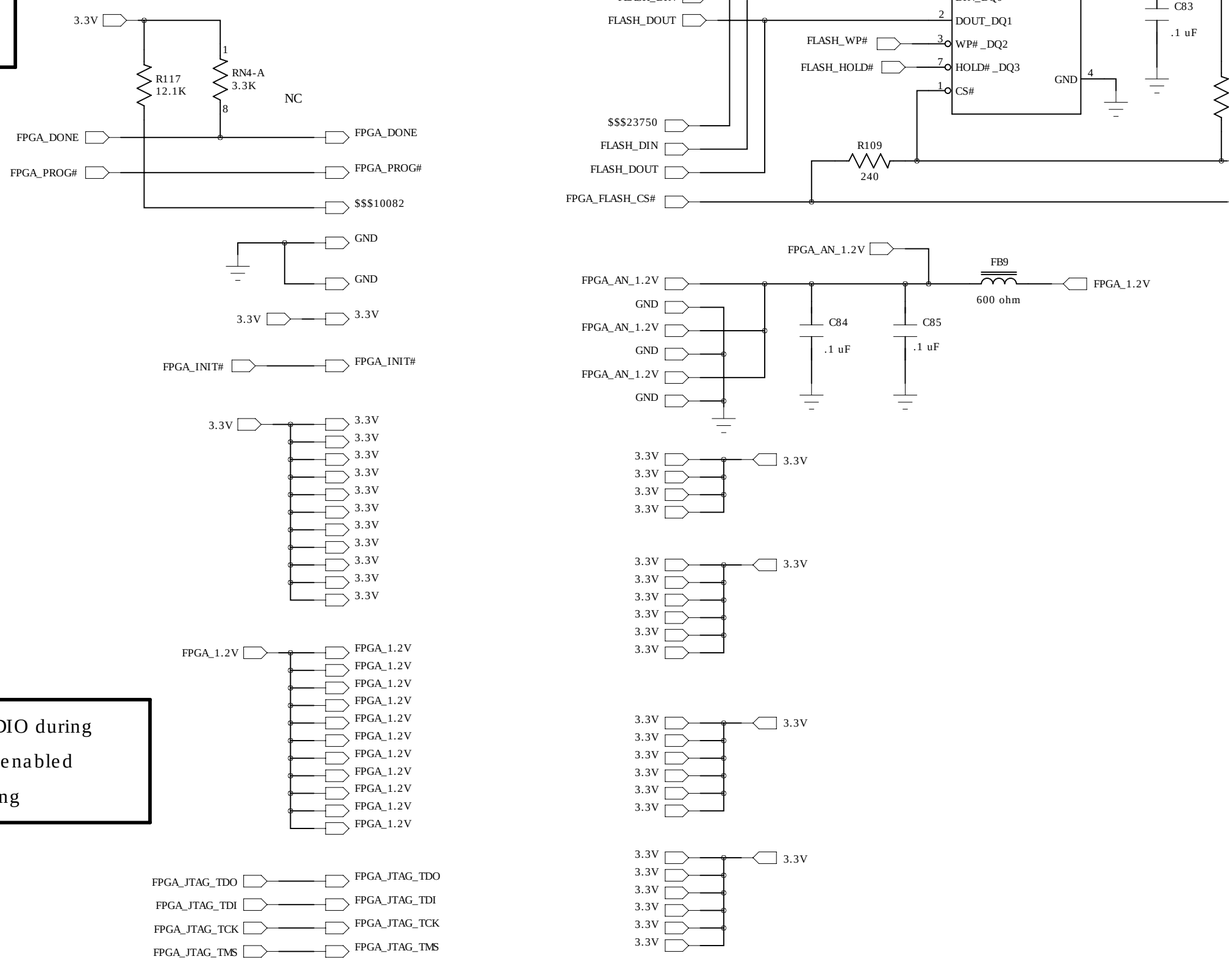


FPGA_INIT# can be used to delay configuration

Also indicates load error

IO_SWAPEN_0 controls DIO during configuration. Low = PU enabled
High = All DIO are floating

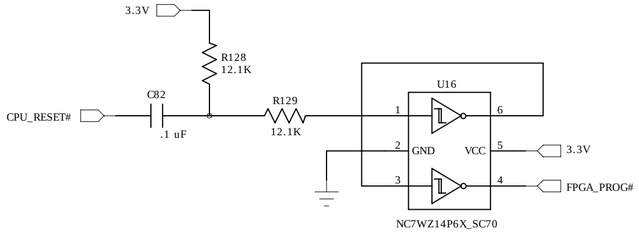
Power and Special Functions

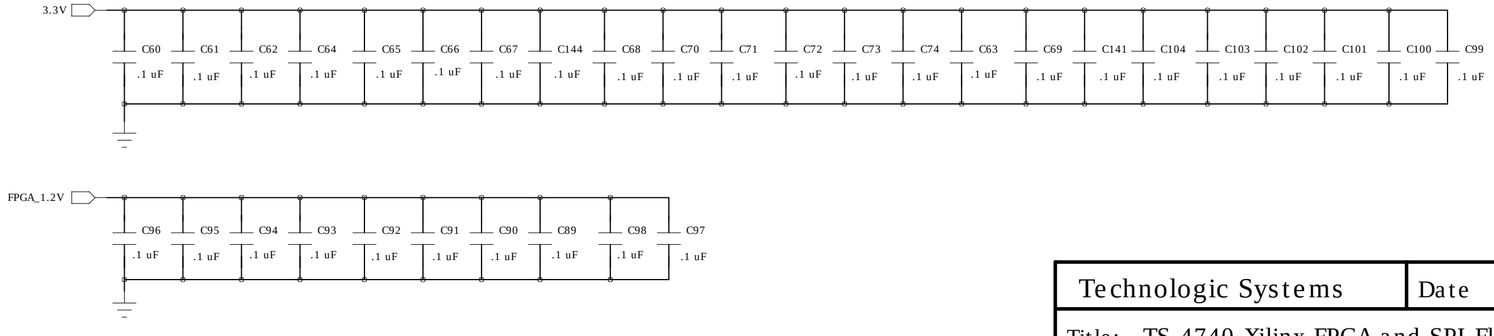


8MB SPI Flash

64 bytes of OTP

FPGA Reload



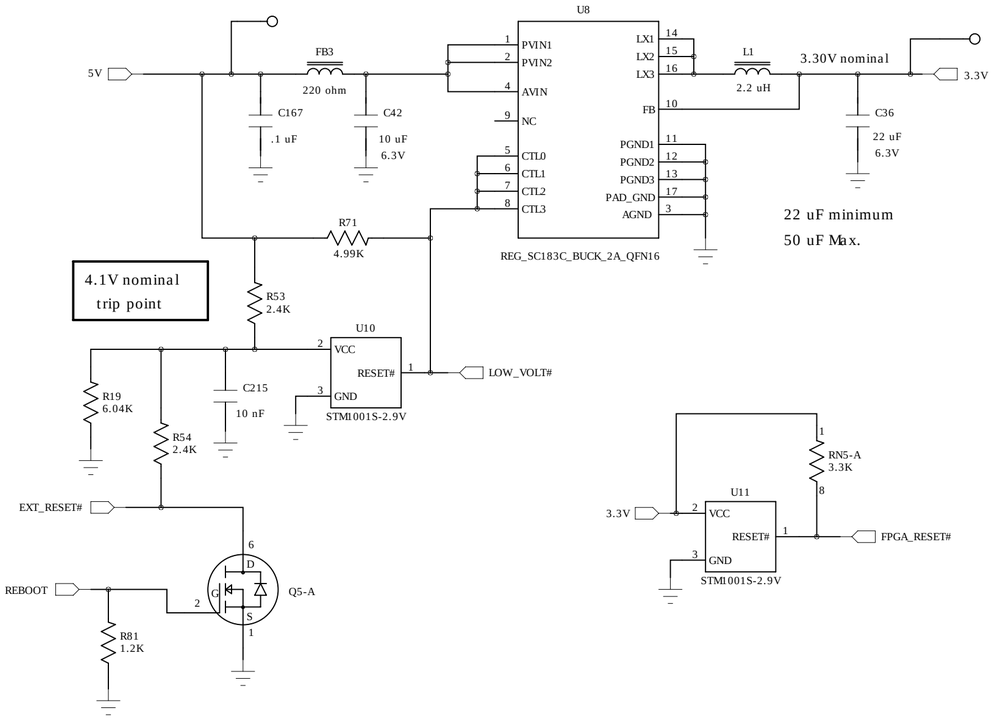


Technologic Systems		Date June 11, 2013
Title: TS-4740 Xilinx FPGA and SPI Flash		
Rev: A	Designer	Sheet 6 of 13

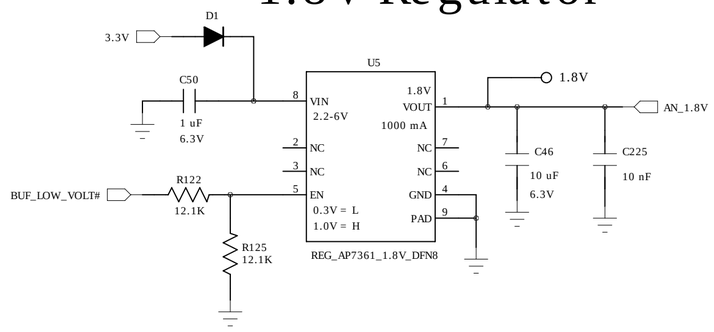
Power Supplies

3.3V Power Supply

up to 2000 mA

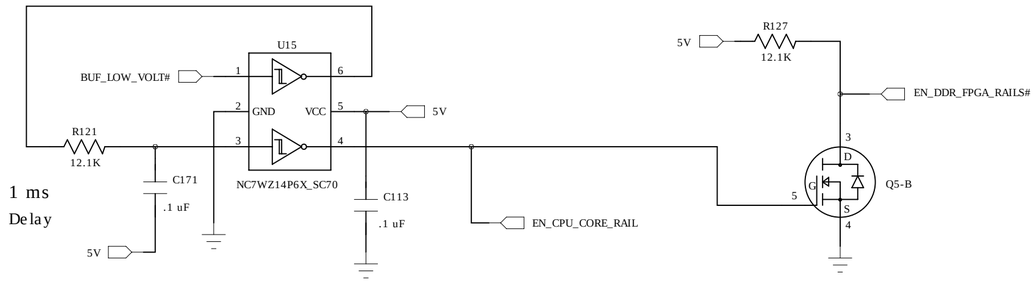


Analog 1.8V Regulator

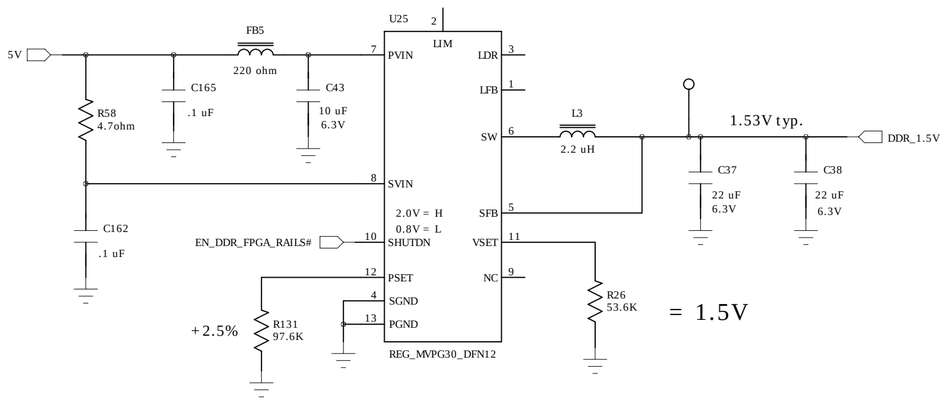


GND

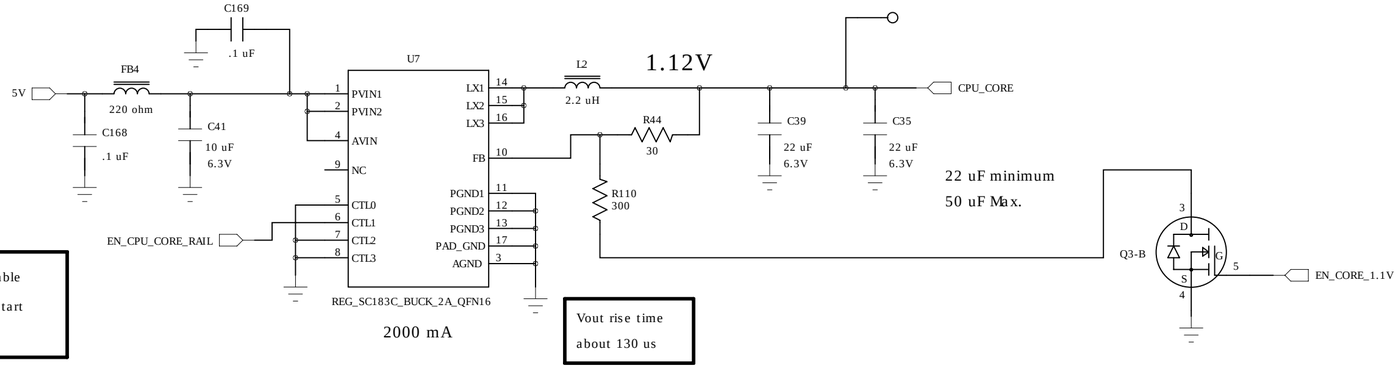
Power Sequencer



DDR3 1.5V Reg.



CPU Core Supply



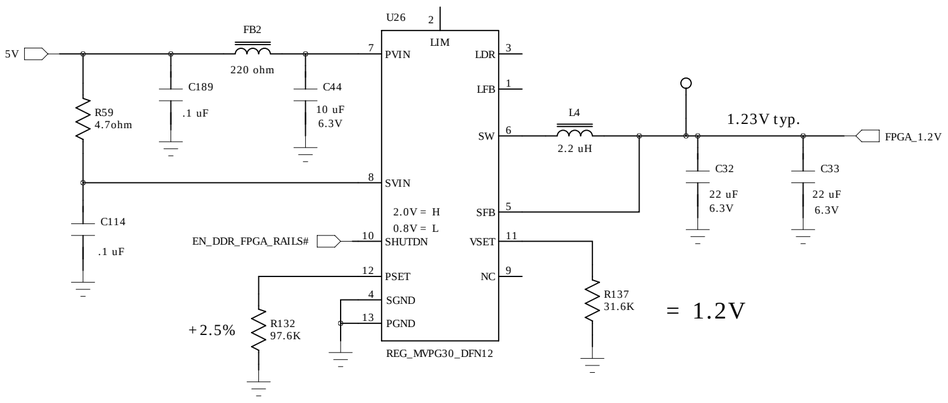
Internal 3 ms delay

Delay from Enable to Vout ramp start is typ. 50 us

Vout rise time about 130 us

Technologic Systems	Date June 11, 2013	
Title: TS-4740 Power Supplies		
Rev: A	Designer	Sheet 7 of 13

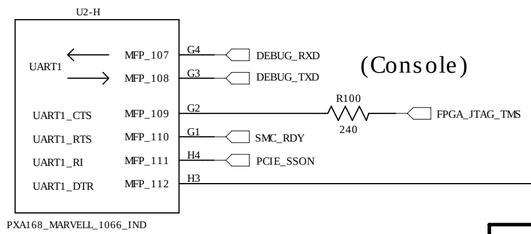
FPGA Core 1.2V



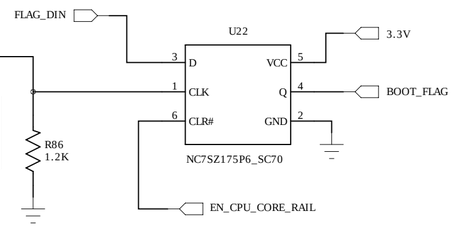
Internal 3 ms delay

CPU

Debug UART



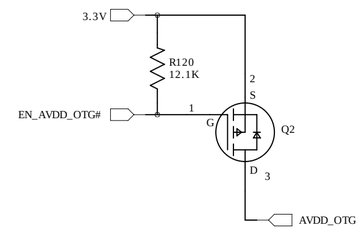
Reboot Flag



Keep normally at logic zero

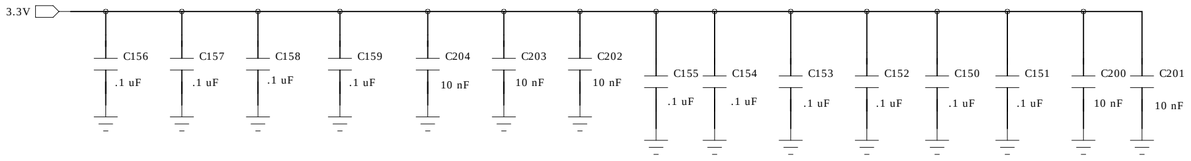
CPU

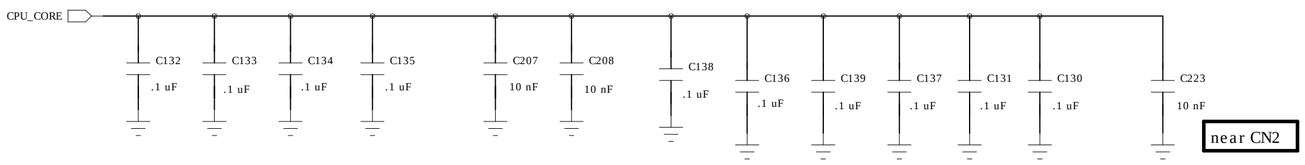
USB Power

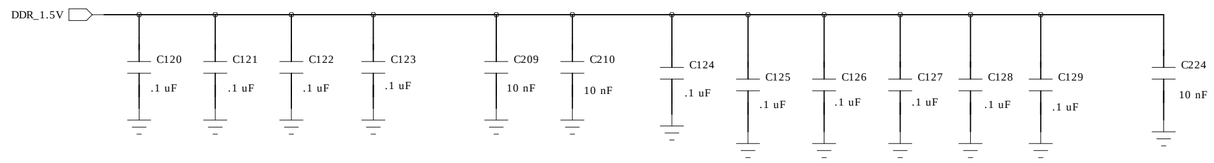


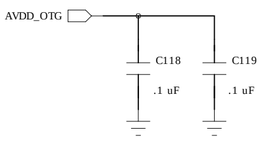
Technologic Systems	Date June 11, 2013	
Title: TS-4740 FPGA 1.2V Supply, Reboot Flag		
Rev: A	Designer	Sheet 8 of 13

CPU Power



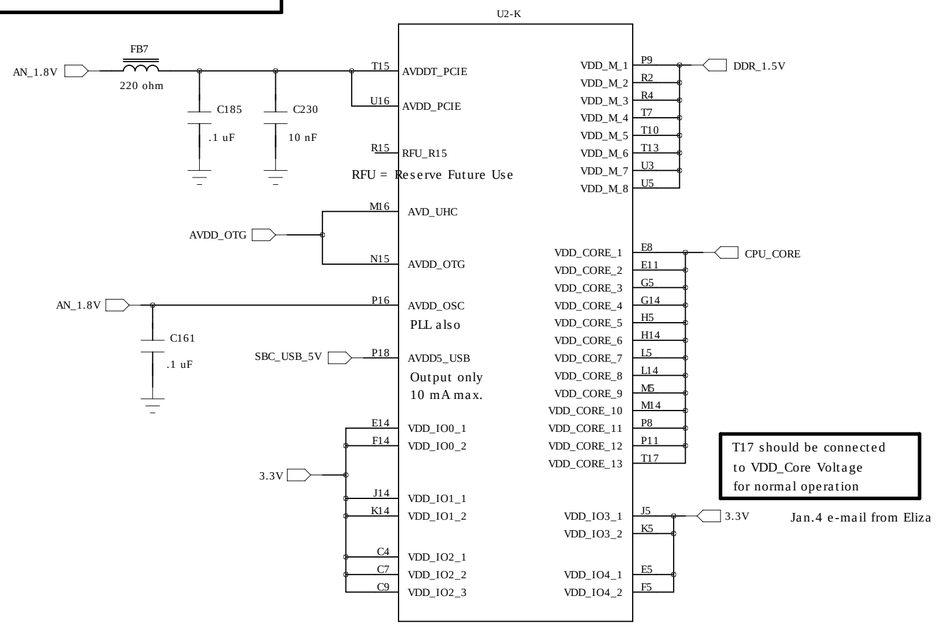




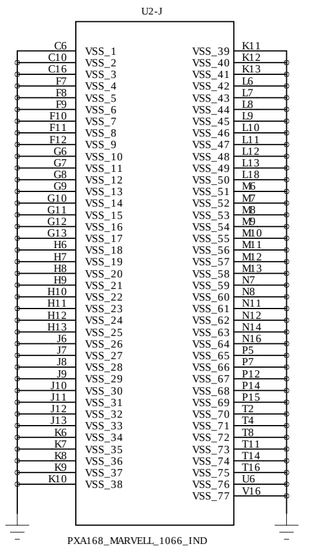


PXA168 PCIE rails must be connected to AN_1.8V

CPU

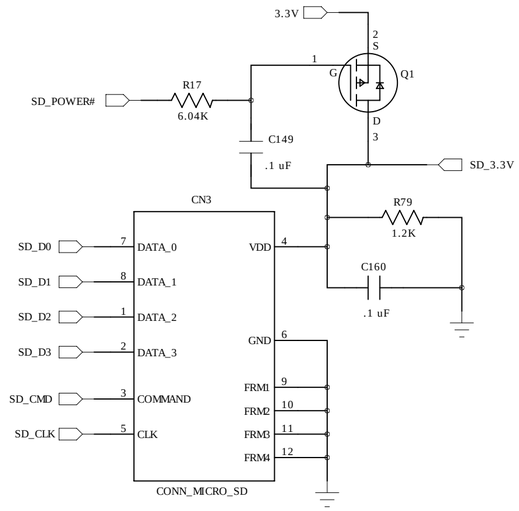


CPU

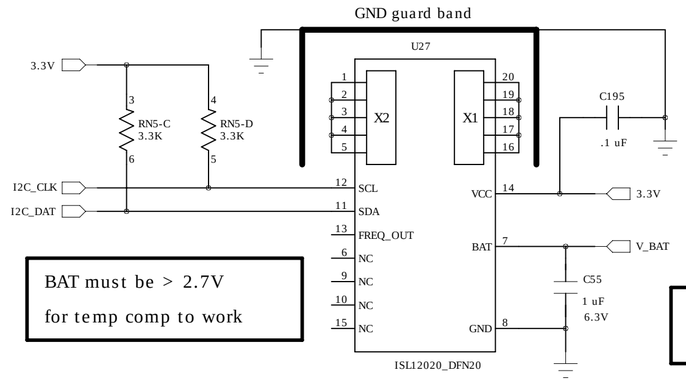


Technologic Systems		Date June 11, 2013
Title: TS-4740 CPU Power and Bypass caps		
Rev: A	Designer	Sheet 9 of 13

Micro SD Card Socket



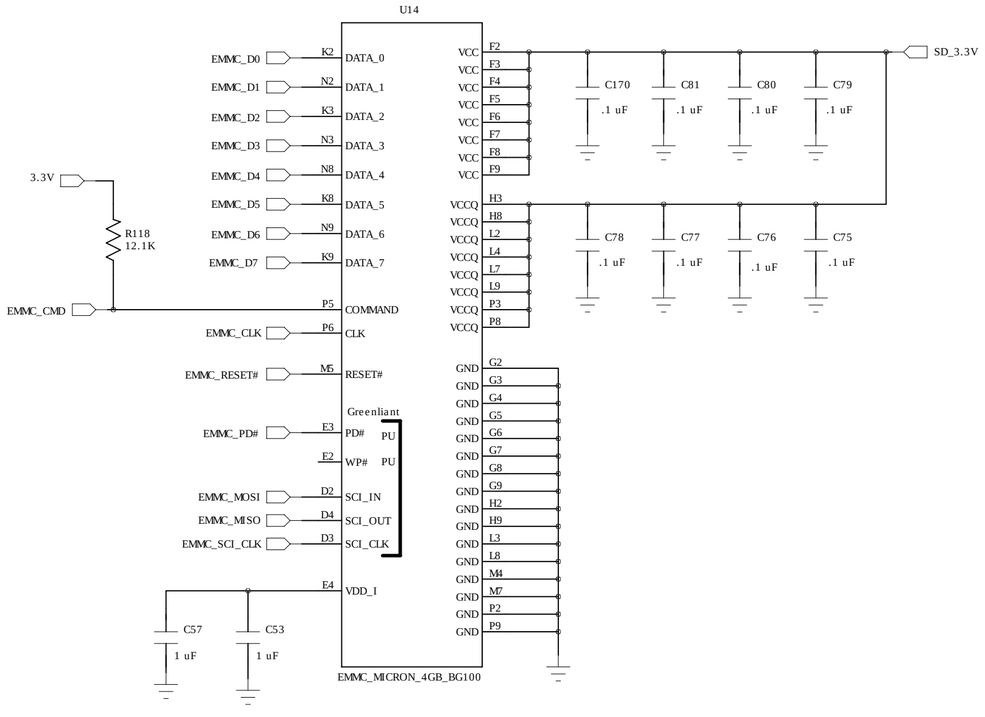
RTC and Temp. Sensor



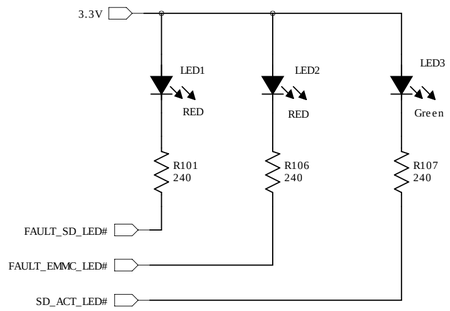
BAT must be > 2.7V
for temp comp to work

Temp takes 68 uA for
22 ms, once every minute

eMMC 4GB

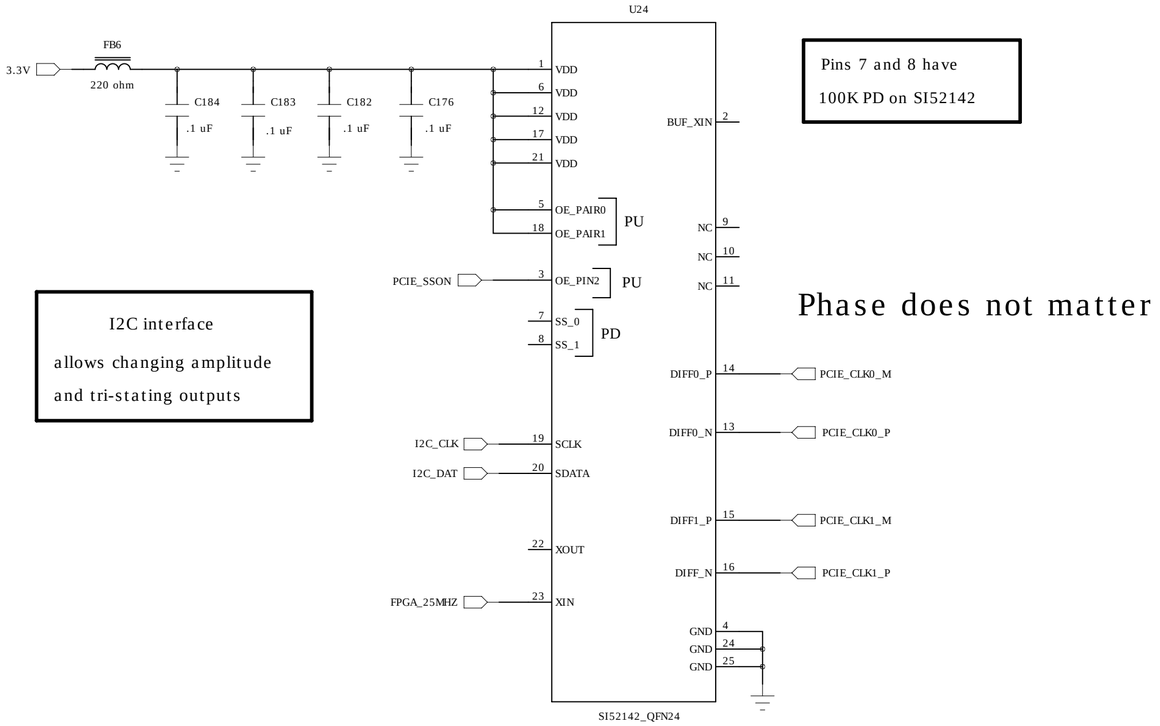


SD Card LEDs



Technologic Systems	Date June 11, 2013	
Title: TS-4740 SD card, eMMC Flash, RTC		
Rev: A	Designer	Sheet 10 of 13

PCIe 100 MHz Clock Generator



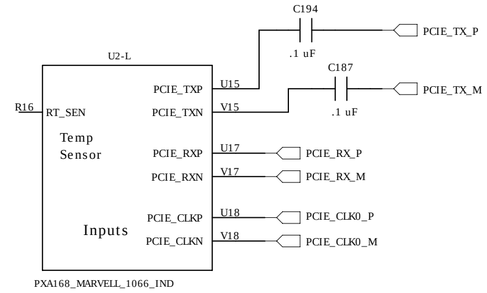
Pins 7 and 8 have
100K PD on SI52142

I2C interface
allows changing amplitude
and tri-stating outputs

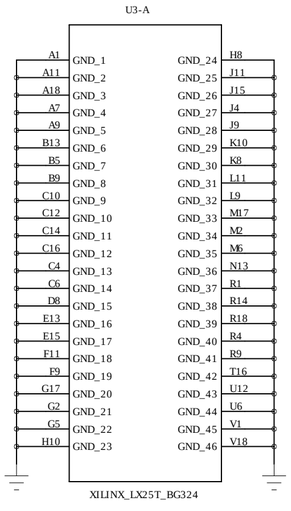
Phase does not matter

CPU PCIe

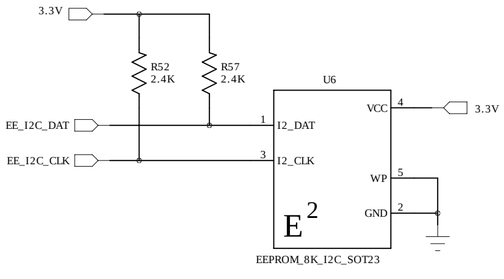
PCIe not supported
on PXA166



FPGA GND



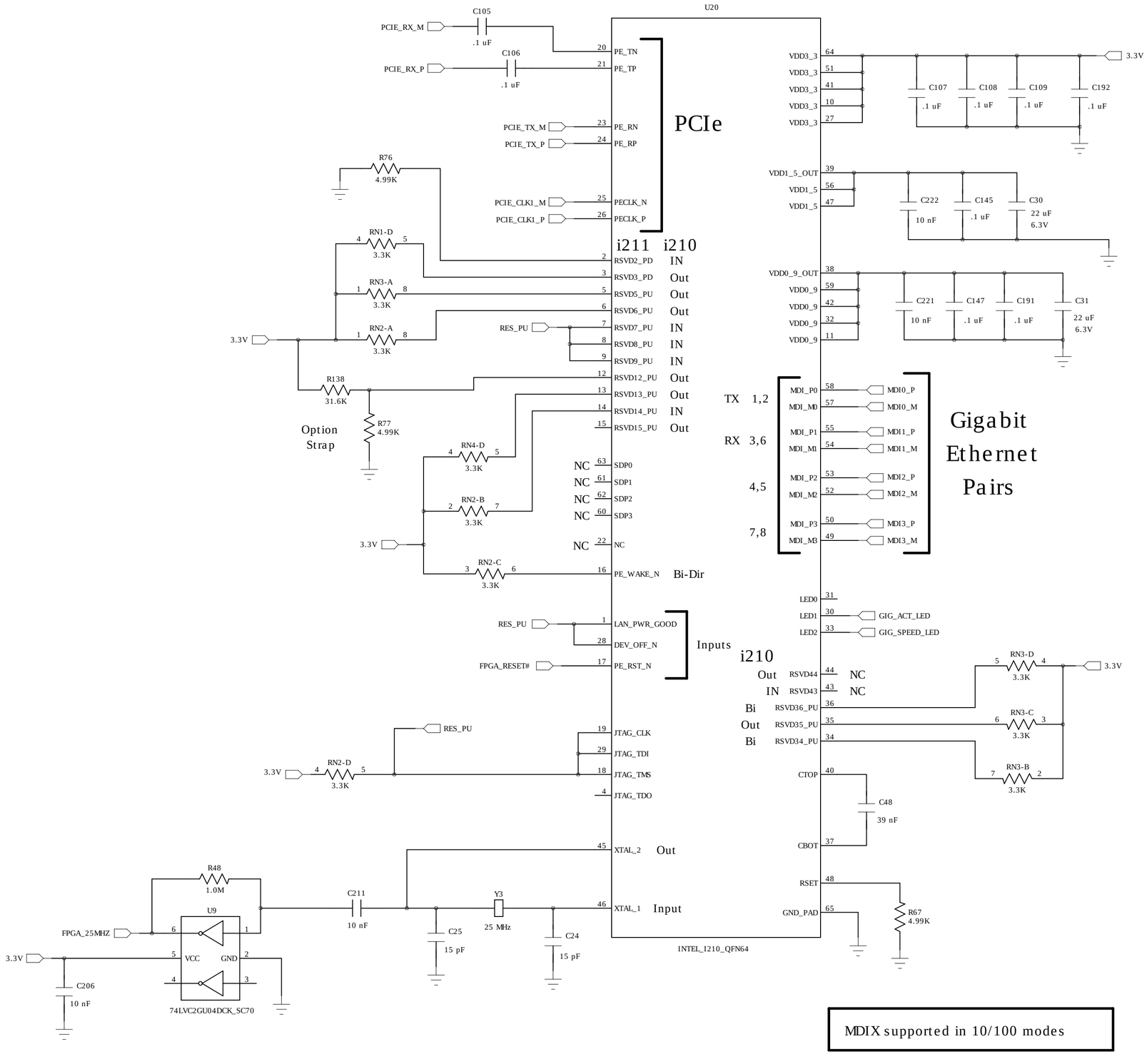
EEPROM 1 Kbyte



I2C address is same as RTC !

Technologic Systems	Date June 11, 2013	
Title: TS-4740 PCIe Clock and CPU PCIe		
Rev: A	Designer	Sheet 11 of 13

Gigabit Ethernet Controller



Technologic Systems	Date June 11, 2013	
Title: TS-4740 Gigabit Ethernet Controller		
Rev: A	Designer	Sheet 12 of 13

Two 100-pin Off-board Connectors

"POWER" pins supply all power to the module
Apply 4.5V to 5.5V to these pins

Current drain is approximately 600 mA

EXT_RESET# is an Input
used to reboot the CPU

Do not drive active high
(use open drain)

All signals driving DIO on CN1 & CN2 must be powered by the 3.3V on CN2, or remain at 0V until the CN2 3.3V rail is > 3.0V

Must have 10 nF Capacitor
very near CN2 and GND
for all "quiet" signals
(between diff pairs)

Pin 1 is the top left corner pin on the connector. All of the pins on the left are odd numbered. This may differ from the connector manufacture's datasheet.

Left

CN1

FPGA JTAG: FPGA_JTAG_TMS 1, FPGA_JTAG_TCK 3, FPGA_JTAG_TDO 5, FPGA_JTAG_TDI 7, OFF_BD_RESET# 9

OFF_BD_RESET# is an Output
used to reset all peripherals

DIO_19 11, DIO_18 13, 15, DIO_17 17, LCD_D08 19, LCD_D09 21, LCD_D10 23, LCD_D11 25, LCD_D12 27, 29, LCD_D13 31, LCD_D14 33, LCD_D15 35, LCD_D16 37, LCD_D17 39, LCD_D18 41, LCD_D19 43, LCD_D20 45, 47, LCD_CLK 49, LCD_HSYNC 51, LCD_VSYNC 53, LCD_DE 55, LCD_PWM 57, FLASH_CS# 59, FPGA_FLASH_CS# 61, 62

5V — C190 .1 uF, C146 .1 uF, C148 .1 uF

EXT_RESET# 2, EN_USB_5V 4, DIO_20 6, DIO_21 8, DIO_22 10, DIO_23 12, DIO_24 14, 16, 5V, DIO_25 18, DIO_26 20, DIO_27 22, LCD_D00 24, LCD_D01 26, LCD_D02 28, LCD_D03 30, LCD_D04 32, LCD_D05 34, 36, V_BAT, C163 .1 uF, LCD_D06 38, LCD_D07 40, LCD_D21 42, LCD_D22 44, LCD_D23 46, EN_LCD_3.3V 48, DIO_28 50, DIO_29 52, DIO_30 54, FLASH_DOUT 56, FLASH_DIN 58, FLASH_CLK 60, 62

DIO_[00:16]

FPGA DIO: DIO_14 63, DIO_13 65, DIO_12 67, DIO_11 69, DIO_10 71, DIO_09 73, 75, DIO_08 77, DIO_07 79, DIO_06 81, DIO_05 83, DIO_04 85, DIO_03 87, DIO_02 89, DIO_01 91, DIO_00 93, 95

Data Bus or DIO: MUX_AD_15 64, MUX_AD_14 66, MUX_AD_13 68, MUX_AD_12 70, MUX_AD_11 72, MUX_AD_10 74, MUX_AD_09 76, MUX_AD_08 78, MUX_AD_07 80, MUX_AD_06 82, MUX_AD_05 84, MUX_AD_04 86, MUX_AD_03 88, MUX_AD_02 90, MUX_AD_01 92, MUX_AD_00 94

Bus Control: BUS_WAIT# 97, BUS_BHE# 99, BUS_ALE# 96, BUS_DIR 98, BUS_CS# 100

MUX_AD_[00:15]

TYCO_100PIN_SBC

Bus Control

If Bus is not needed, all Bus signals can be changed to DIO

Devices connected to this bus must never drive it when BUS_CS# is deasserted
(must be off within 30 nS of deassertion)

Devices must pull the BUS_WAIT# line low if they need more than 150 nS strobe

Right

CN2

Gigabit Ethernet: MDI0_P 1, MDI0_M 3, GIG_CT 5, MDI1_P 7, MDI1_M 9, GIG_CT 11, 3.3V 13, 15, MDI2_P 17, MDI2_M 19, 21, MDI3_P 23, MDI3_M 25

3.3V rail can supply up to 700 mA to base board

Maximum off-board load on AN_1.8V is 10 mA

USB Ports: HOSTA_USB_M 27, HOSTA_USB_P 29, CPU_CORE 31, USB_OTG_M 33, USB_OTG_P 35, 37, 39

3.3V — C213 10 nF

41, 43, 45, 47, 49, 51, 53, 55, 57, 59

DDR_1.5V — C217 10 nF

SPI or DIO: AN_1.8V 61, SPI_FRM 63, SPI_MOSI 65, SPI_MISO 67, SPI_CLK 69

CPU JTAG Vcc: 3.3V 71

Max. load on JTAG_Vcc (CN2-79) is 20 mA
Not always 3.3V

Camera or DIO: CAM_D3 73, CAM_D4 75, CAM_PCLK 77, CAM_VCLK 79, MFP_52 81, MFP_43 83

Console: DEBUG_TXD 85, DEBUG_RXD 87

CAN: DIO_15 89, DIO_16 91

DIO_15 and DIO_16 can be CAN_TXD and CAN_RXD

TYCO_100PIN_SBC

GIG_ACT_LED 2, GIG_SPEED_LED 4, RED_LED# 6, GREEN_LED# 8, FE_ACT_LED 10, MFP_106 12, MFP_122 14

MFP_122 = PWM3

FE Ethernet Port: FE_RX_P 16, FE_RX_M 18, FE_CT 20, FE_TX_P 22, FE_TX_M 24

MFP_49 26

I2C: I2C_CLK 28, I2C_DAT 30

MFP_104 32

MFP_104 = PWM4

I2S or DIO: AUD_MCLK 34, AUD_CLK 36, AUD_FRM 38, AUD_TXD 40, AUD_RXD 42

CPU JTAG: CPU_JTAG_TMS 44, CPU_JTAG_TCK 46, CPU_JTAG_TDI 48, CPU_JTAG_TDO 50

CN2-54 Codec CLK on the TS-8390

ONE_WIRE 52, MFP_51 54

MFP_51 has FPGA pin in parallel
** Can use either

Camera or DIO: CAM_MCLK 56, CAM_D0 58, CAM_D1 60, CAM_D2 62, CAM_D5 64, CAM_D6 66, CAM_D7 68, CAM_HSYNC 70, CAM_VSYNC 72

USB_OTG_ID 74, USB_5V_LINE 76

Serial Ports or DIO: UART0_TXD 78, UART0_RXD 80, UART1_TXD 82, UART1_RXD 84, UART2_TXD 86, UART2_RXD 88, UART3_TXD 90, UART3_RXD 92, UART4_TXD 94, UART4_RXD 96, UART5_TXD 98, UART5_RXD 100

GIG_CT — C115 .1 uF — near CN2-5

Any I/O routed to a user accessible connector should have additional ESD protection placed on the carrier board.

Technologic Systems	Date June 11, 2013	
Title: TS-4740 Off-board Connectors		
Rev: A	Designer	Sheet 13 of 13