TS-4900 iMX6 SBC

Options

XOPP1 — NC — ASSEMBLY_OPTIONS

Option 2	TS-4900-1024-S10S-C	Single core, 1 GHz, no WiFi, no RTC, no eMMC, 1GByte RAM, (0 to 70)
Option 3	TS-4900-1024-4096F-S8S-RTC-I	Single core, 800 MHz, no WiFi, 1 GByte RAM (-40 to 85)
Option 4	TS-4900-1024-4096F-S8S-RTC-WIFI-I	Single core, 800 MHz, with WiFi, 1 GByte RAM (-40 to 85)
Option 5	TS-4900-2048-4096F-Q10S-RTC-E	Quad core, 1 GHz, no WiFi, 2GByte RAM, (Temp -20 to 85)
Option 6	TS-4900-2048-4096F-Q10S-RTC-WIFI-E	Quad core, 1 GHz, with WiFi, 2GByte RAM, (Temp -20 to 85)

Rev.A --> Rev.C Changes

Moved parts and copper away from mounting holes

Par interface pins were swapped
U4.K23 and U4.H21 = CN1 pins 65 and 99

Biased BOOT_MODE_1 high
and BOOT_MODE_0 low

5 LVDS diff pairs connected to CN2

CN2 pins 56, 58 and 60 go to different CPU DIO

Audio MCLK changed to CN2-54

CPU JTAG signals no longer connected to CN2
CPU JTAG signals go to Test Points

Rev.D changes:

Allow external PCIe 100 MHz CLK
No layout change needed - BOM change

Added 4mm keep out around iMX6
top layer for new heat sink

Changed to 153-ball eMMC

Added EIM Byte strobe to CN1 pin 22
FPGA ball "P4" controls SD power

Allow FPGA to be 1-time programmed
For Windows CE applications
Requires PU on FPGA_SPI_CS#
Also connect to CN2 pin 34

Ball "L6" on CPU is GND, to indicate Rev.D

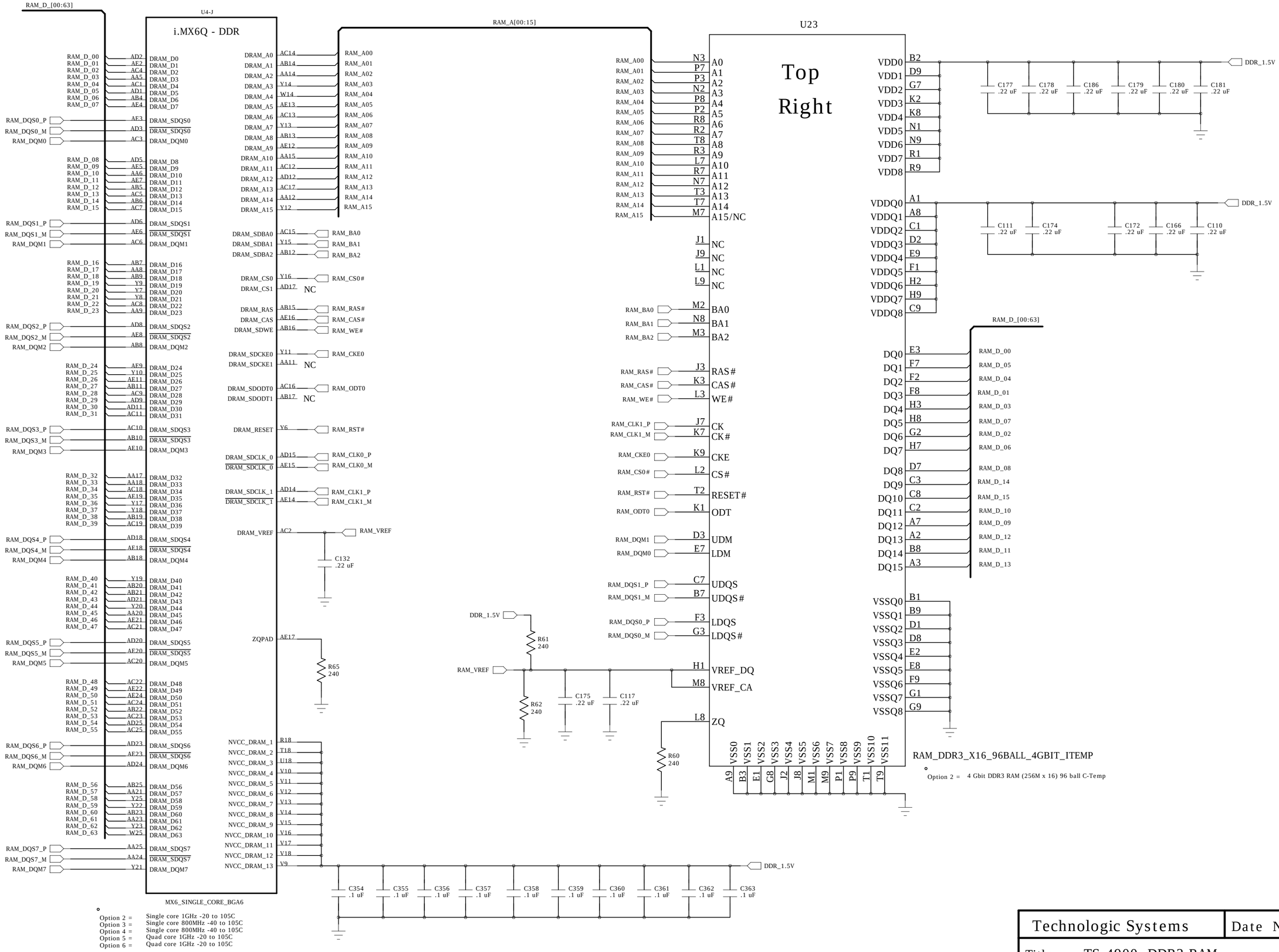
JTAG ball "H6" is GND

CN1 pin 12 is wrong, but can't change it

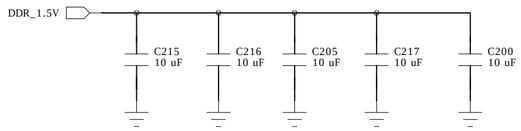
Web Schematic: Some proprietary information has been withheld.

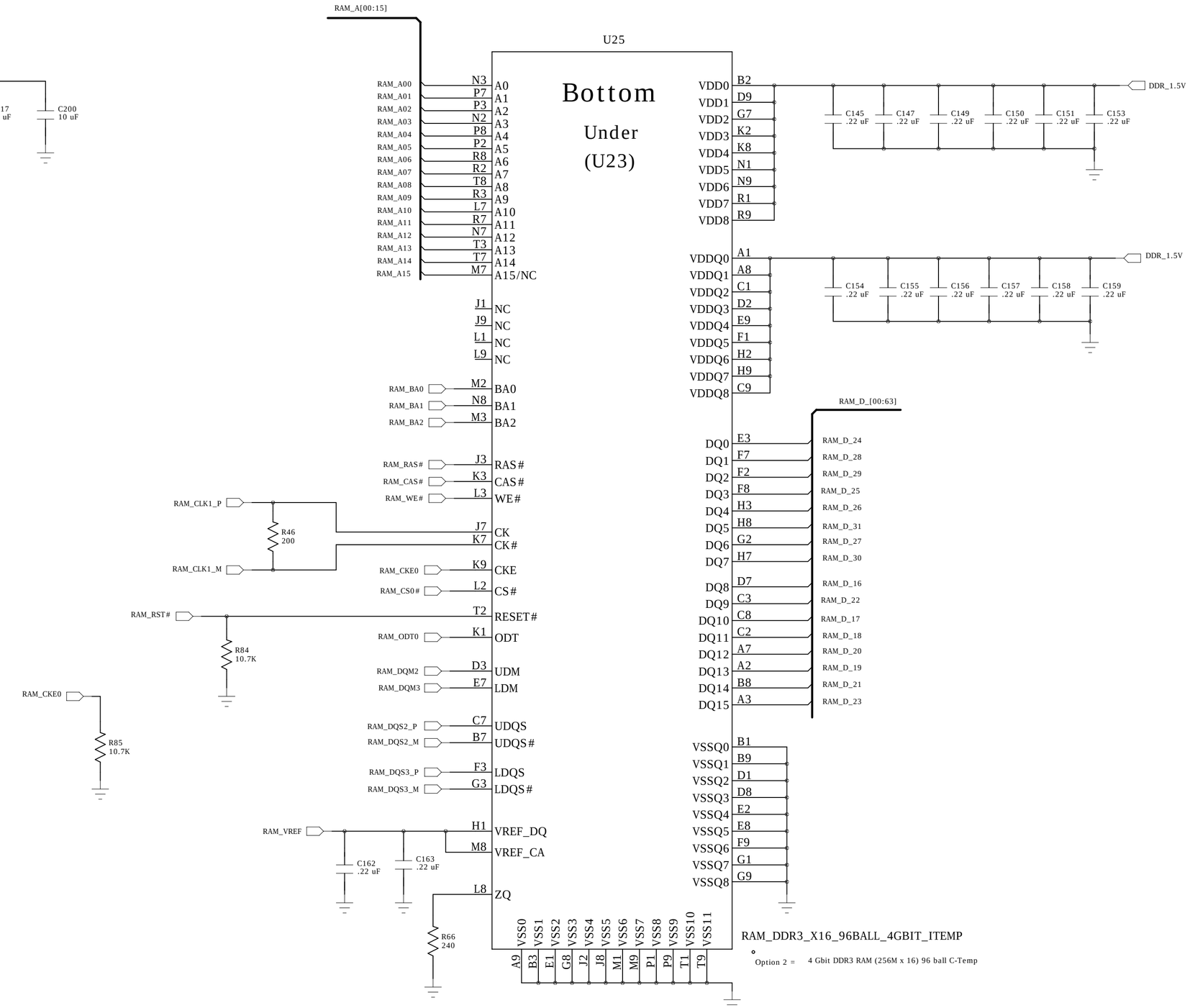
Technologic Systems		Date Nov. 19, 2015
Title: TS-4900 MX6 SBC		
Rev: D	Designer	Sheet 0 of 15

512 MB per RAM Chip



Technologic Systems	Date Nov. 19, 2015	
Title: TS-4900 DDR3 RAM		
Rev: D	Designer	Sheet 2 of 15

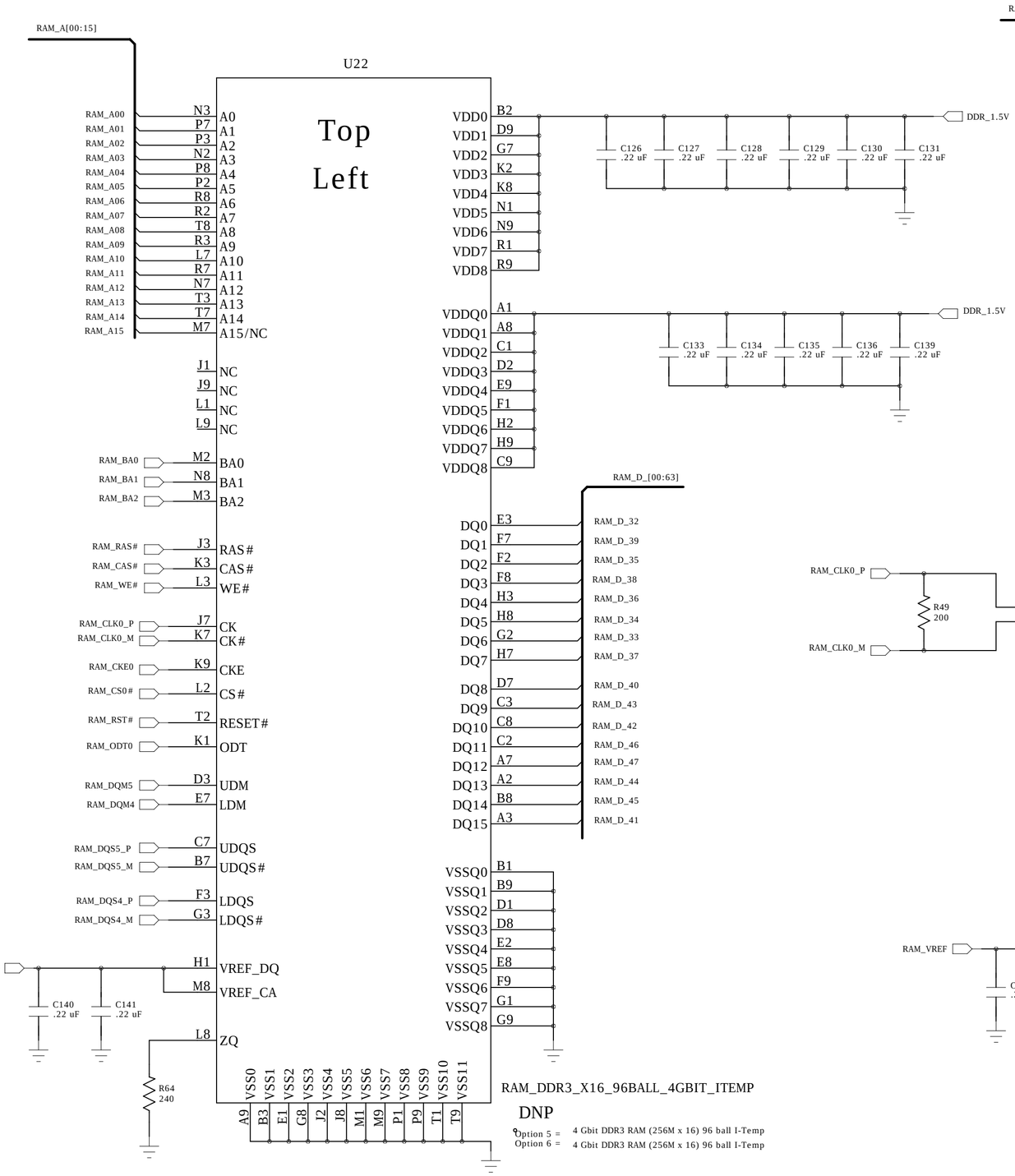


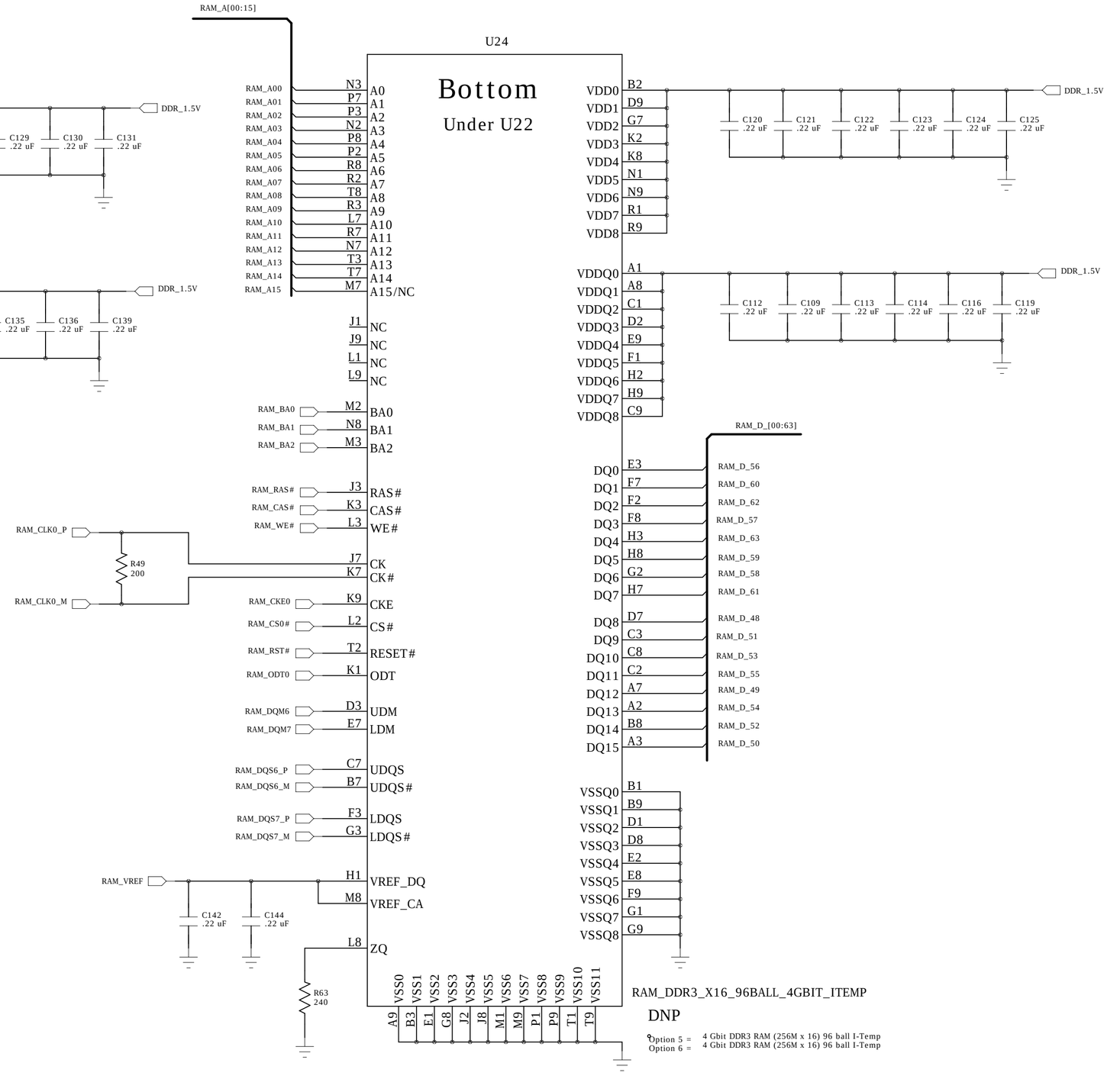


Technologic Systems		Date Nov. 19, 2015
Title: TS-4900 DDR3 RAM		
Rev: D	Designer	Sheet 3 of 15

RAM Data bits 32-63

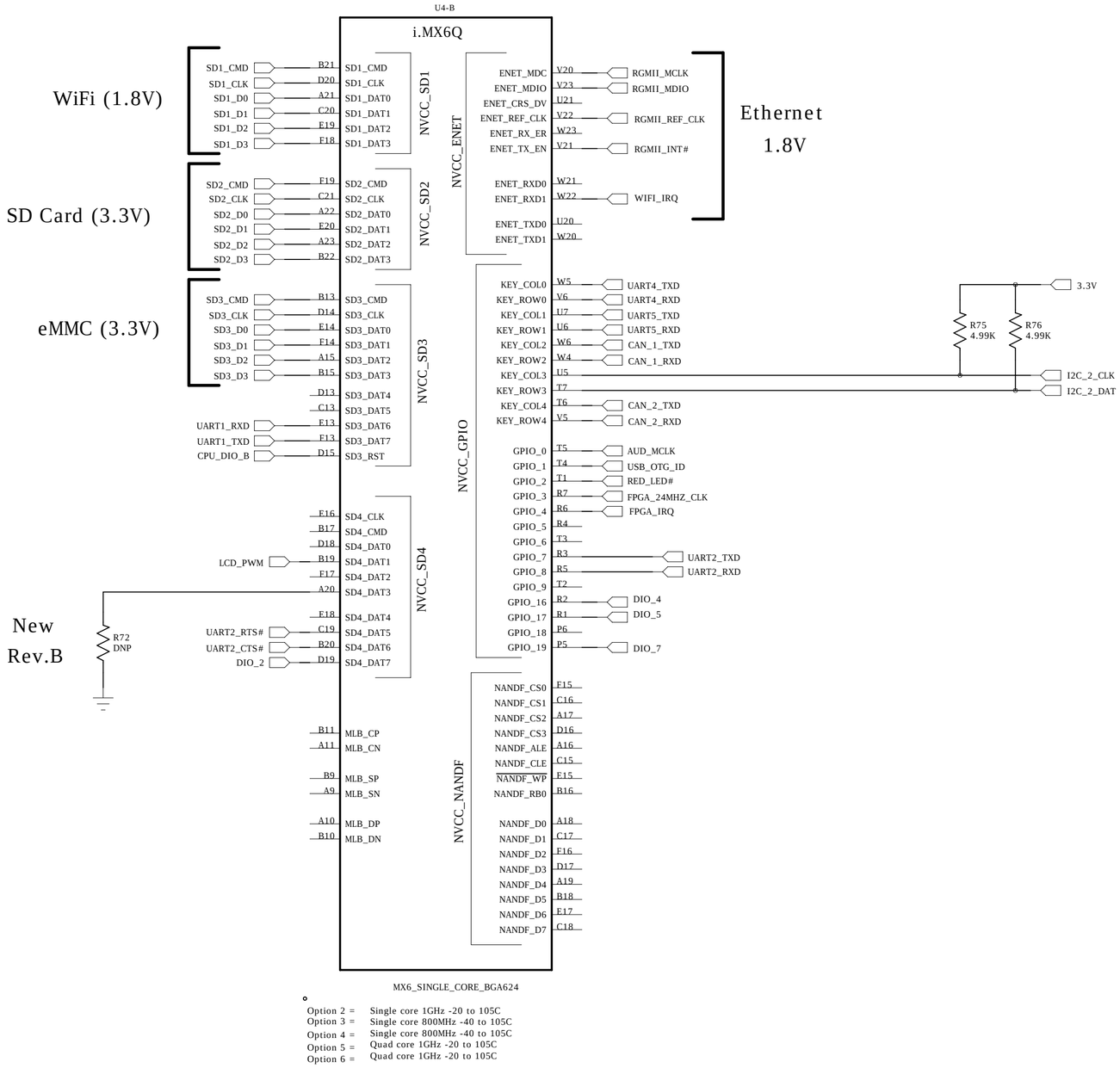
Not populated for Single Core CPU



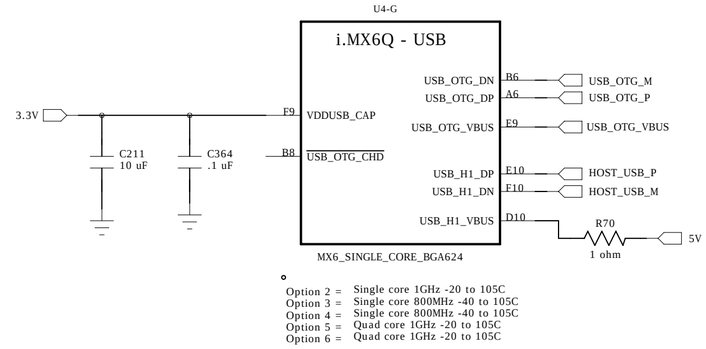


Technologic Systems	Date Nov. 19, 2015	
Title: TS-4900 DDR3 RAM		
Rev: D	Designer	Sheet 4 of 15

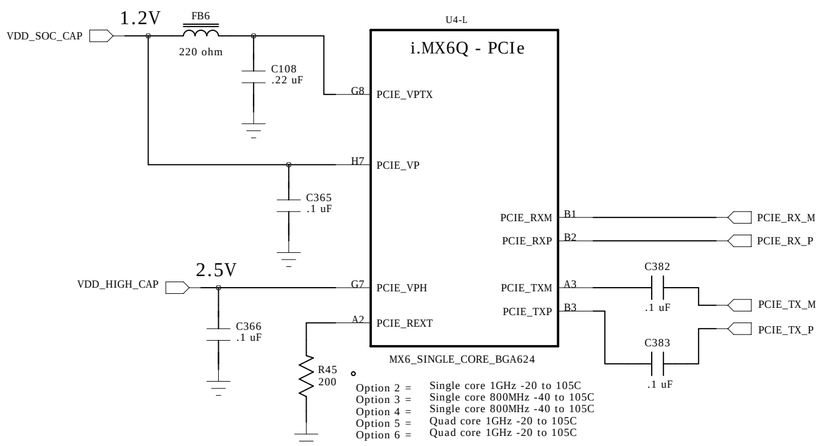
SD, GPIO, NAND



USB



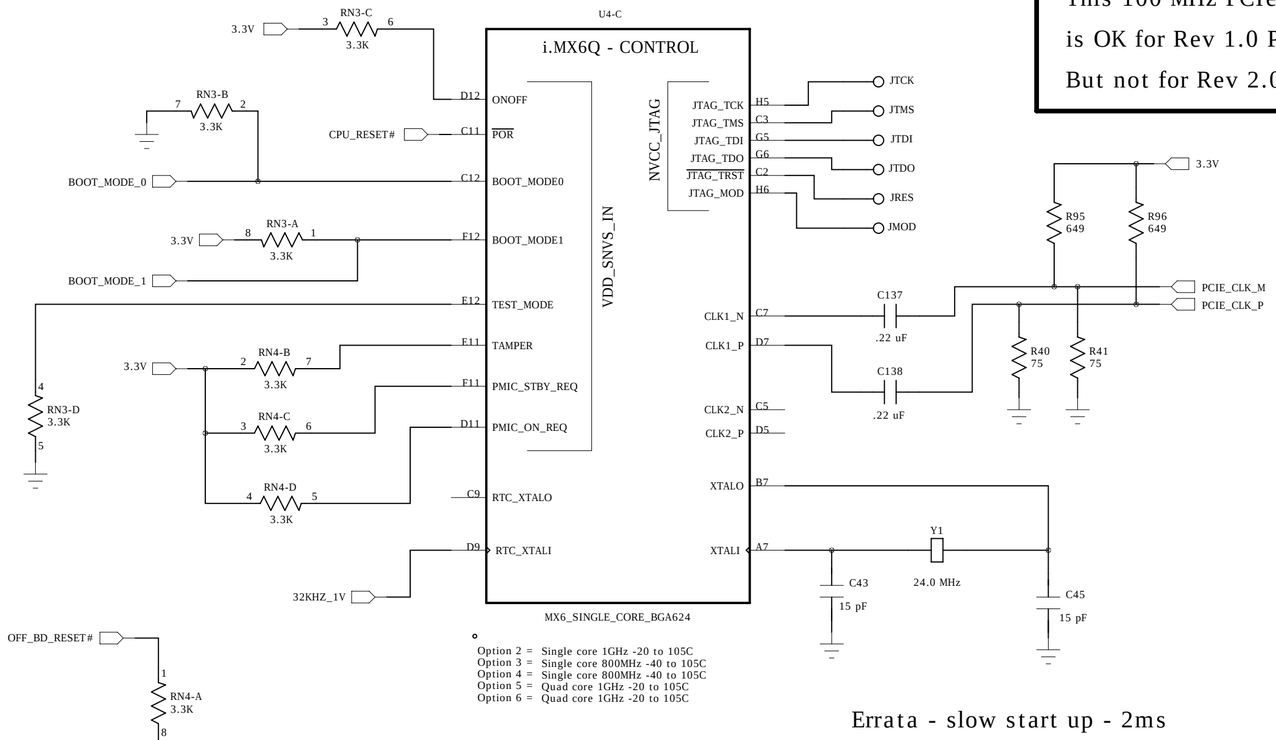
PCIe



Technologic Systems	Date Nov. 19, 2015	
Title: TS-4900 MX6 SBC		
Rev: D	Designer	Sheet 6 of 15

Control

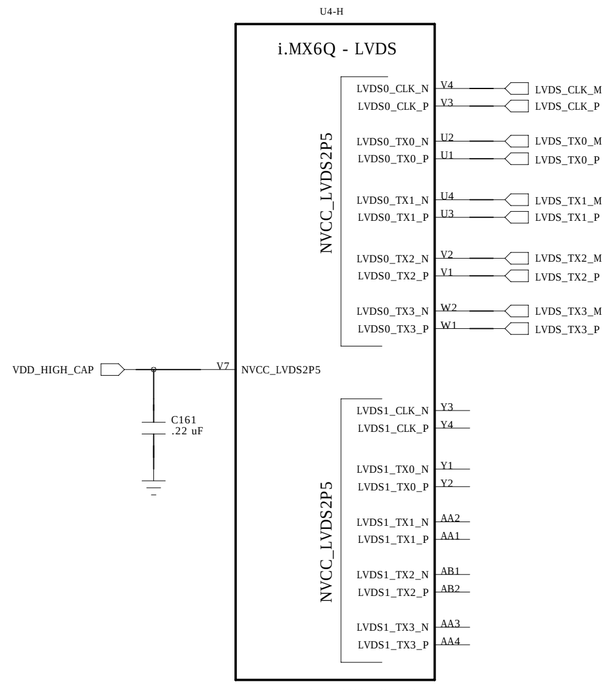
This 100 MHz PCIe clock
is OK for Rev 1.0 PCIe
But not for Rev 2.0



Option 2 = Single core 1GHz -20 to 105C
Option 3 = Single core 800MHz -40 to 105C
Option 4 = Single core 800MHz -40 to 105C
Option 5 = Quad core 1GHz -20 to 105C
Option 6 = Quad core 1GHz -20 to 105C

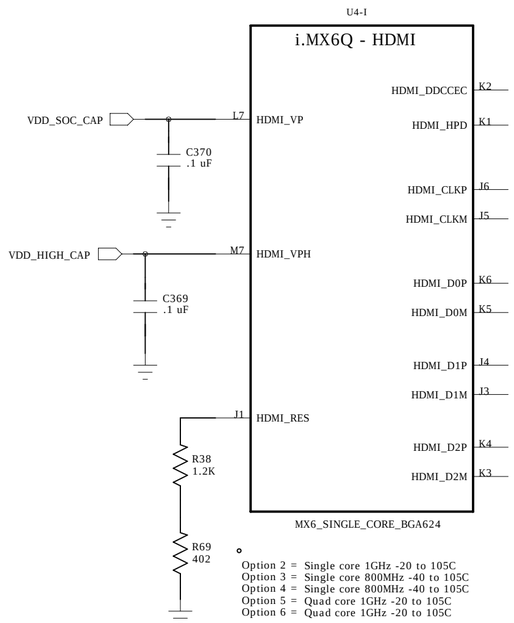
Errata - slow start up - 2ms

LVDS



Option 2 = Single core 1GHz -20 to 105C
Option 3 = Single core 800MHz -40 to 105C
Option 4 = Single core 800MHz -40 to 105C
Option 5 = Quad core 1GHz -20 to 105C
Option 6 = Quad core 1GHz -20 to 105C

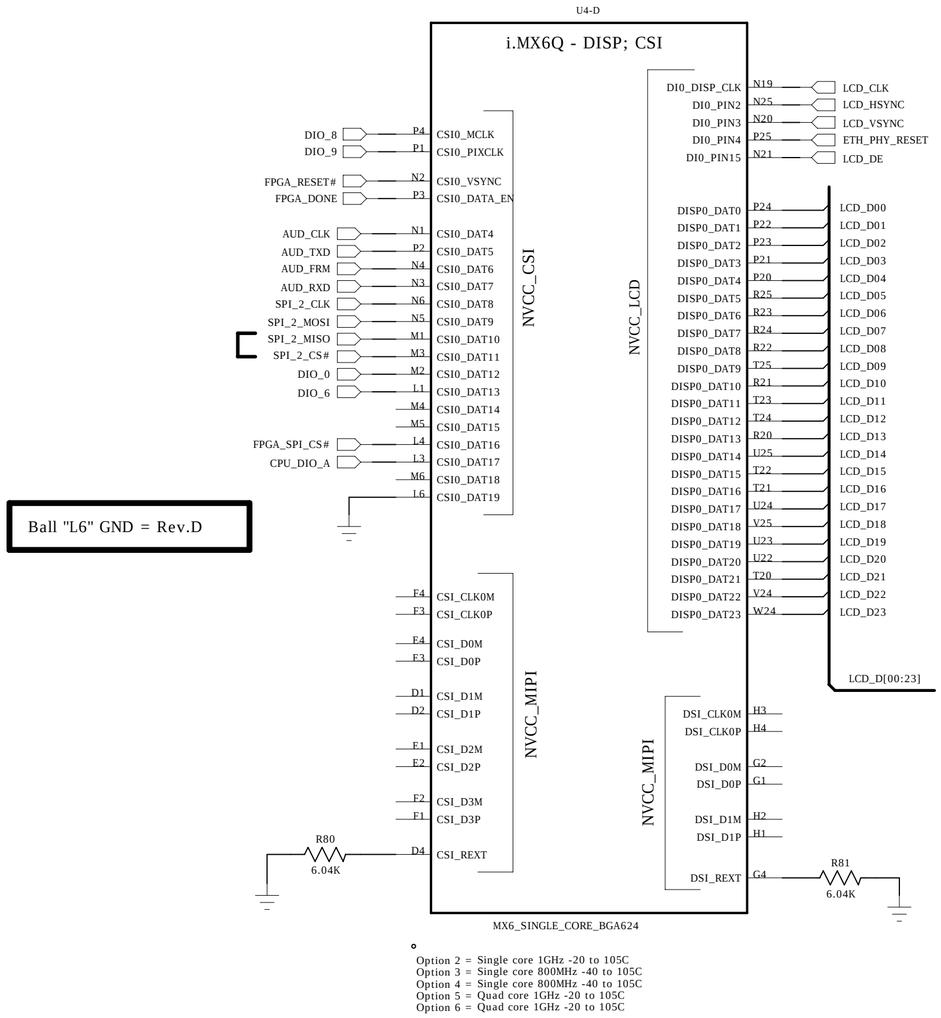
HDMI



Option 2 = Single core 1GHz -20 to 105C
Option 3 = Single core 800MHz -40 to 105C
Option 4 = Single core 800MHz -40 to 105C
Option 5 = Quad core 1GHz -20 to 105C
Option 6 = Quad core 1GHz -20 to 105C

Technologic Systems	Date Nov. 19, 2015	
Title: TS-4900		
Rev: D	Designer	Sheet 7 of 15

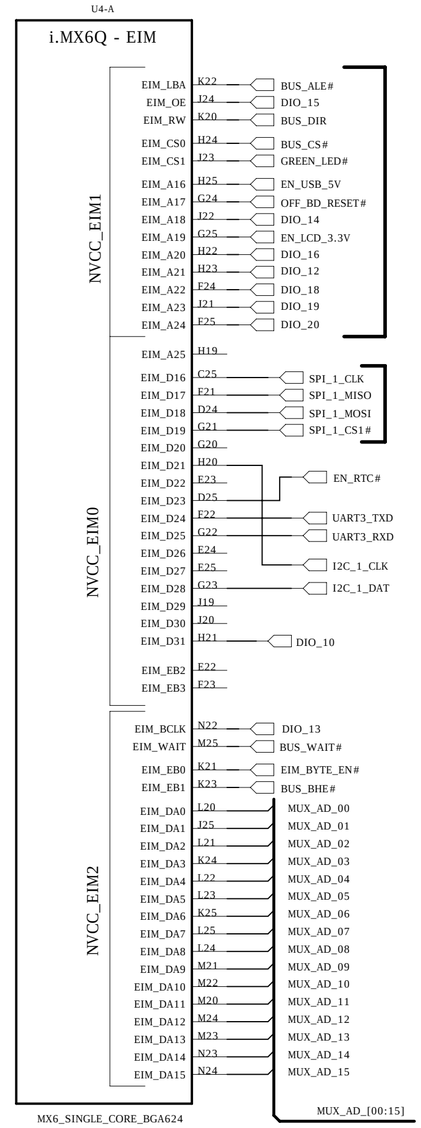
LCD



Ball "L6" GND = Rev.D

Option 2 = Single core 1GHz -20 to 105C
Option 3 = Single core 800MHz -40 to 105C
Option 4 = Single core 800MHz -40 to 105C
Option 5 = Quad core 1GHz -20 to 105C
Option 6 = Quad core 1GHz -20 to 105C

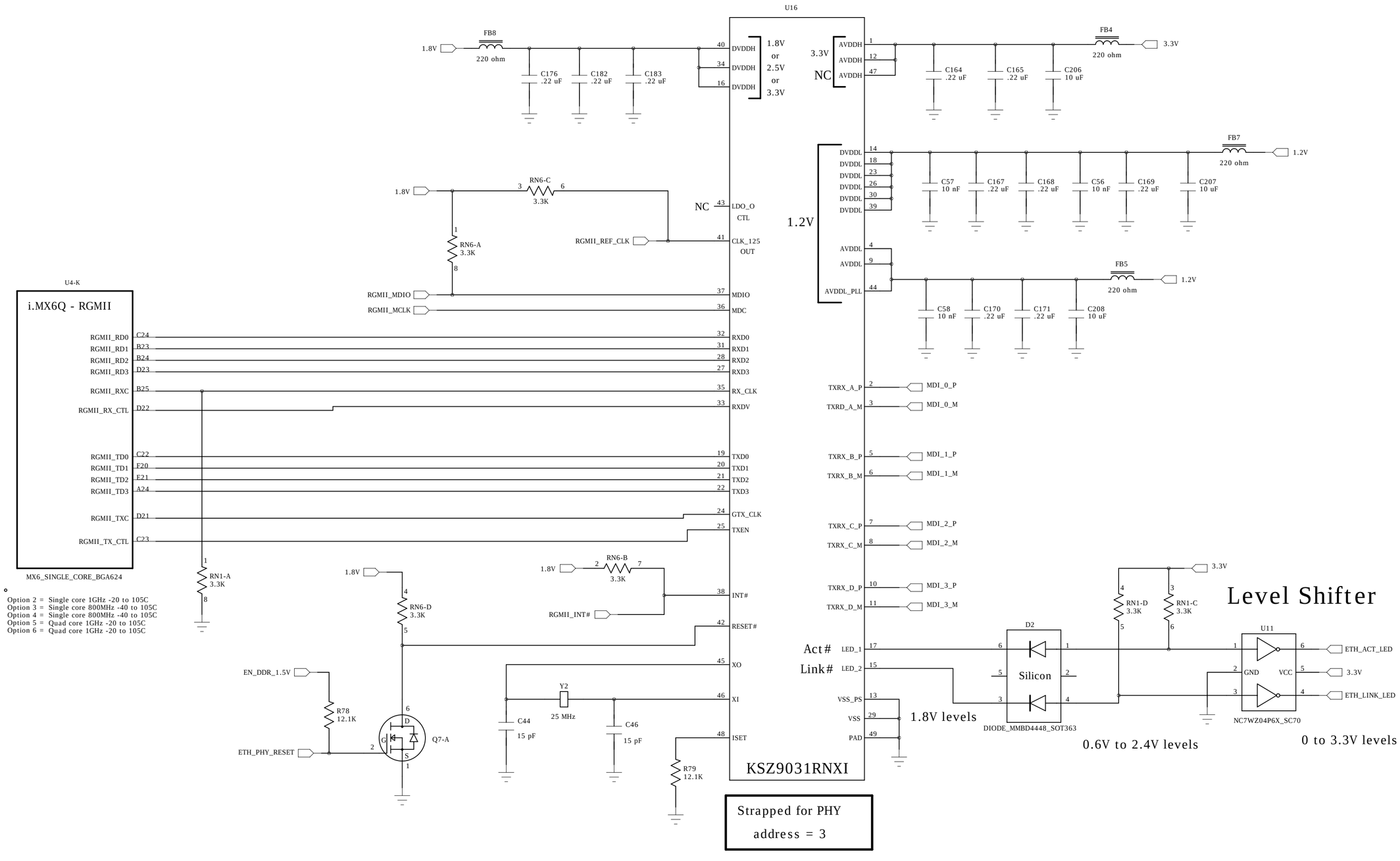
EIM



Option 2 = Single core 1GHz -20 to 105C
Option 3 = Single core 800MHz -40 to 105C
Option 4 = Single core 800MHz -40 to 105C
Option 5 = Quad core 1GHz -20 to 105C
Option 6 = Quad core 1GHz -20 to 105C

Technologic Systems	Date Nov. 19, 2015	
Title: TS-4900 LCD signals		
Rev: D	Designer	Sheet 8 of 15

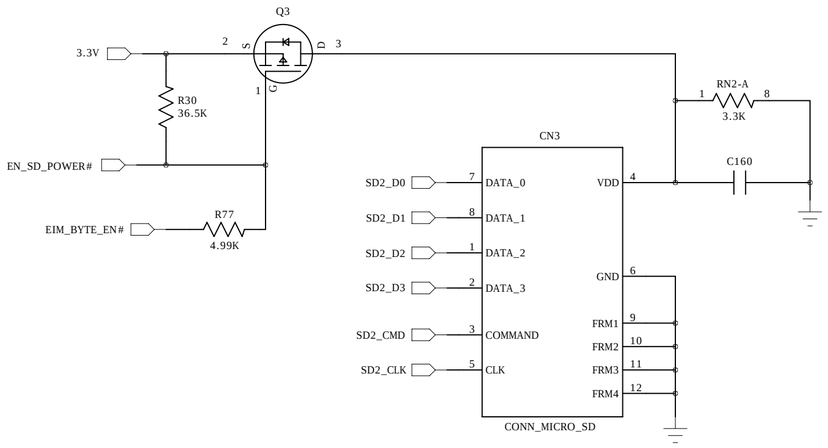
10/100/1000 Ethernet PHY



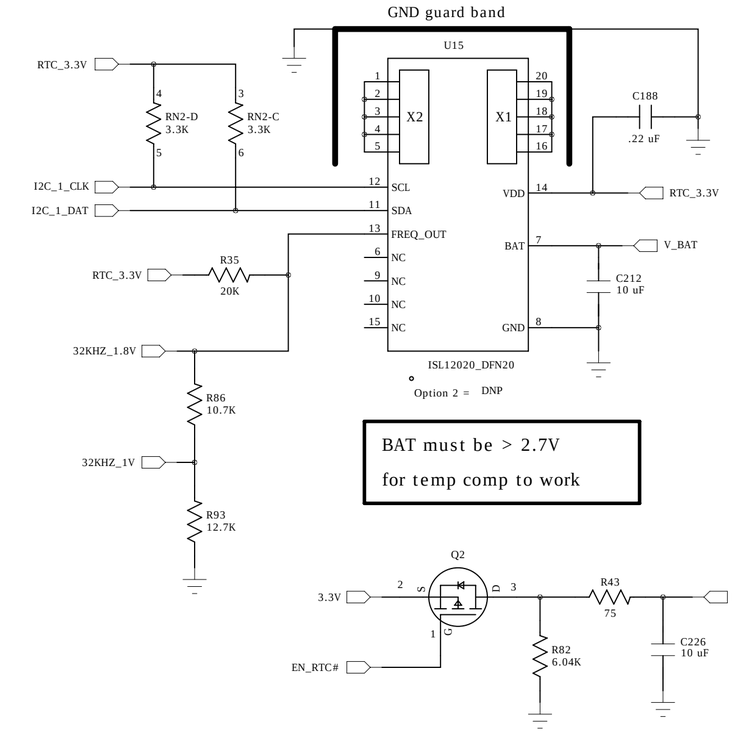
Option 2 = Single core 1GHz -20 to 105C
Option 3 = Single core 800MHz -40 to 105C
Option 4 = Single core 800MHz -40 to 105C
Option 5 = Quad core 1GHz -20 to 105C
Option 6 = Quad core 1GHz -20 to 105C

Technologic Systems		Date Nov. 19, 2015
Title: TS-4900 Gigabit Ethernet PHY		
Rev: D	Designer RLM	Sheet 9 of 15

Micro SD Card Socket



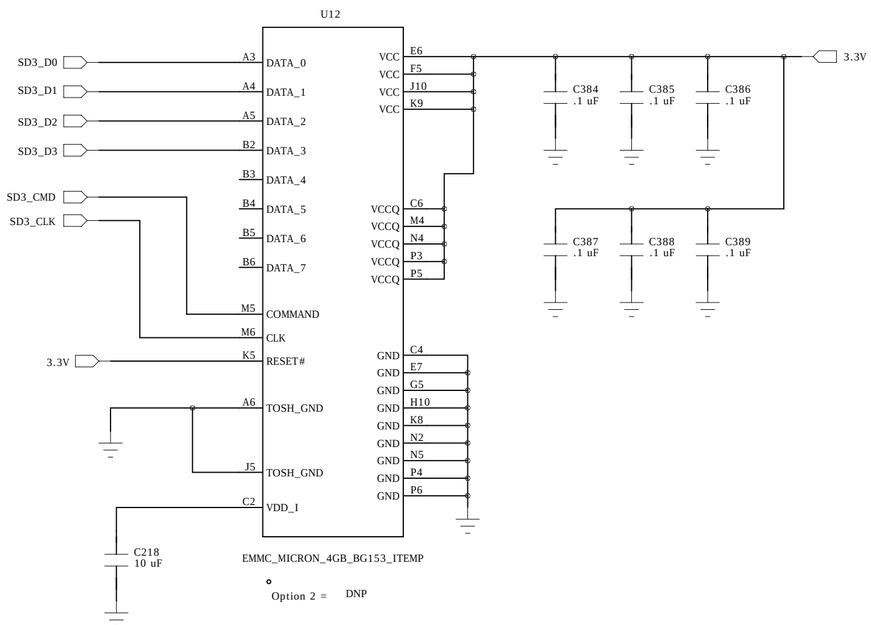
RTC and Temp. Sensor



BAT must be > 2.7V
for temp comp to work

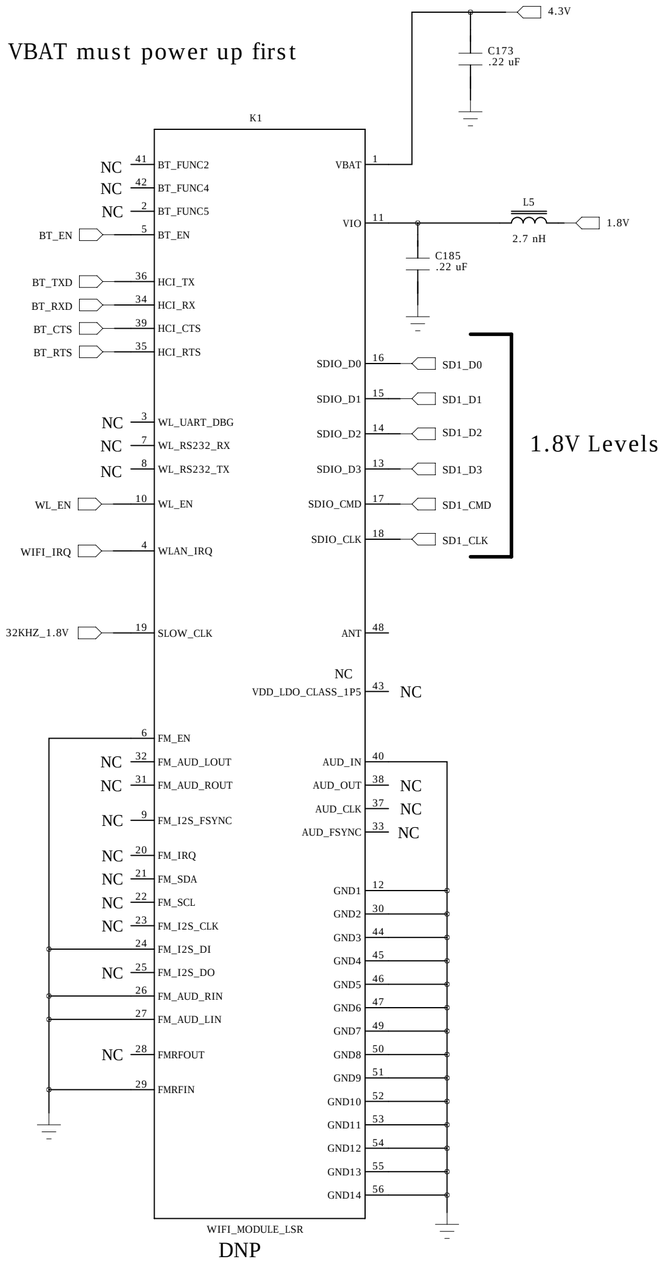
EN_RTC# has weak PU on CPU DIO
At system power up, FET is off

eMMC 4GB



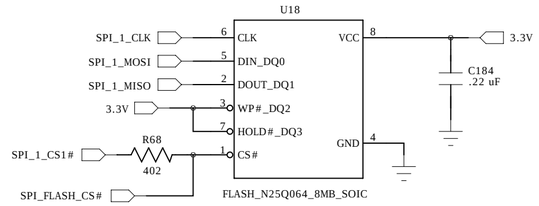
Technologic Systems		Date Nov. 19, 2015
Title: TS-4900 SD card, RTC, Temp.		
Rev: D	Designer	Sheet 12 of 15

WiFi Radio



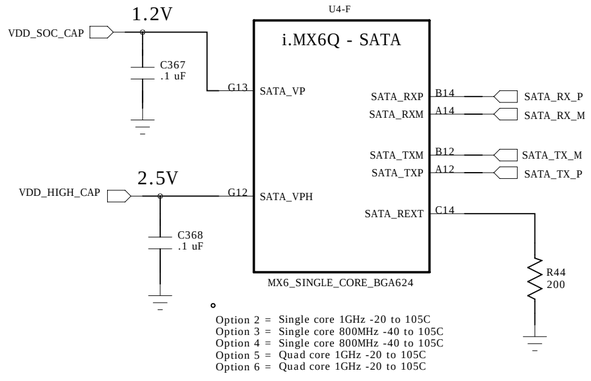
° Option 4 = LS Research TiWi-BLE SDIO WiFi 802.11BGN and Bluetooth 4.0
Option 6 = LS Research TiWi-BLE SDIO WiFi 802.11BGN and Bluetooth 4.0

SPI Boot Flash



64 bytes of OTP

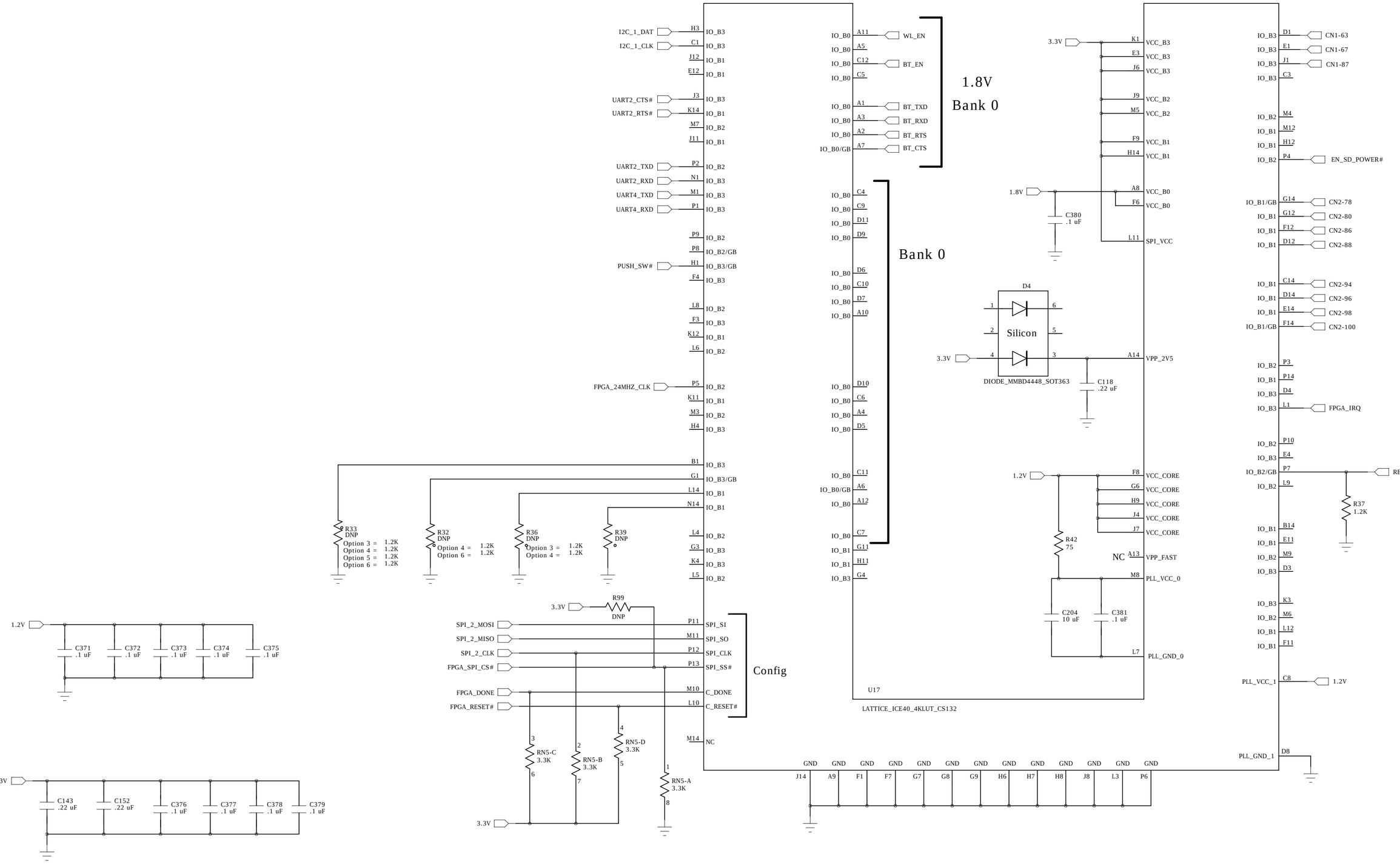
SATA



° Option 2 = Single core 1GHz -20 to 105C
Option 3 = Single core 800MHz -40 to 105C
Option 4 = Single core 800MHz -40 to 105C
Option 5 = Quad core 1GHz -20 to 105C
Option 6 = Quad core 1GHz -20 to 105C

Technologic Systems		Date Nov. 19, 2015
Title: TS-4900 WiFi		
Rev: D	Designer	Sheet 13 of 15

iCE40 FPGA



Technologic Systems		Date Nov. 19, 2015
Title: TS-4900 iCE40 FPGA		
Rev: D	Designer	Sheet 14 of 15

Two 100-pin Off-board Connectors

"5V" pins supply all power to the module
Apply 4.5V to 5.5V to these pins

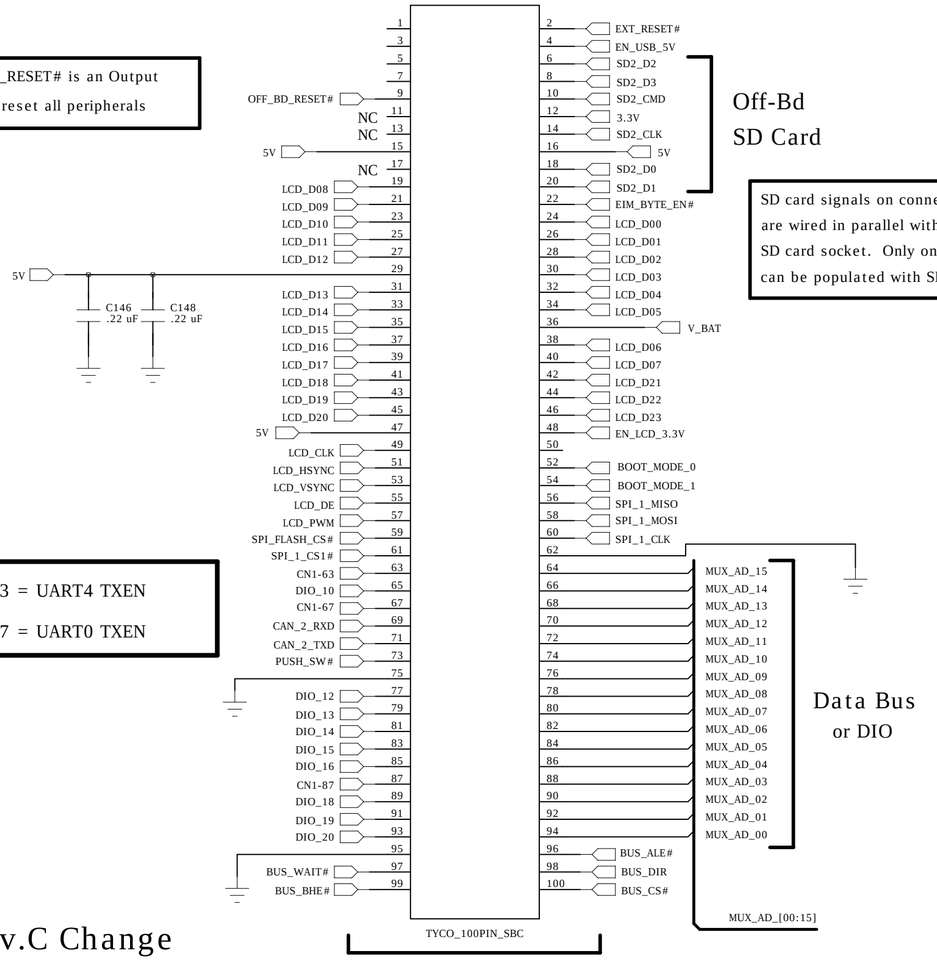
OFF_BD_RESET# is an Output
used to reset all peripherals

EXT_RESET# is an Input
used to reboot the CPU

Do not drive active high
(use open drain)

Left

CN1



Off-Bd
SD Card

SD card signals on connector
are wired in parallel with
SD card socket. Only one
can be populated with SD card

Data Bus
or DIO

Bus Control

CN1-Pin 63 = UART4 TXEN

CN1-Pin 67 = UART0 TXEN

Rev.C Change

CN1-65 (DIO_10) and CN1-99
were swapped on CPU

If Bus is not needed, all Bus
signals can be changed to DIO

⚠ Any I/O routed to a user accessible connector should have additional ESD protection placed on the carrier board.

⚠ All signals driving DIO on CN1 & CN2 must be powered by the 3.3V on CN2, or remain at 0V until the CN2 3.3V rail is > 3.0V

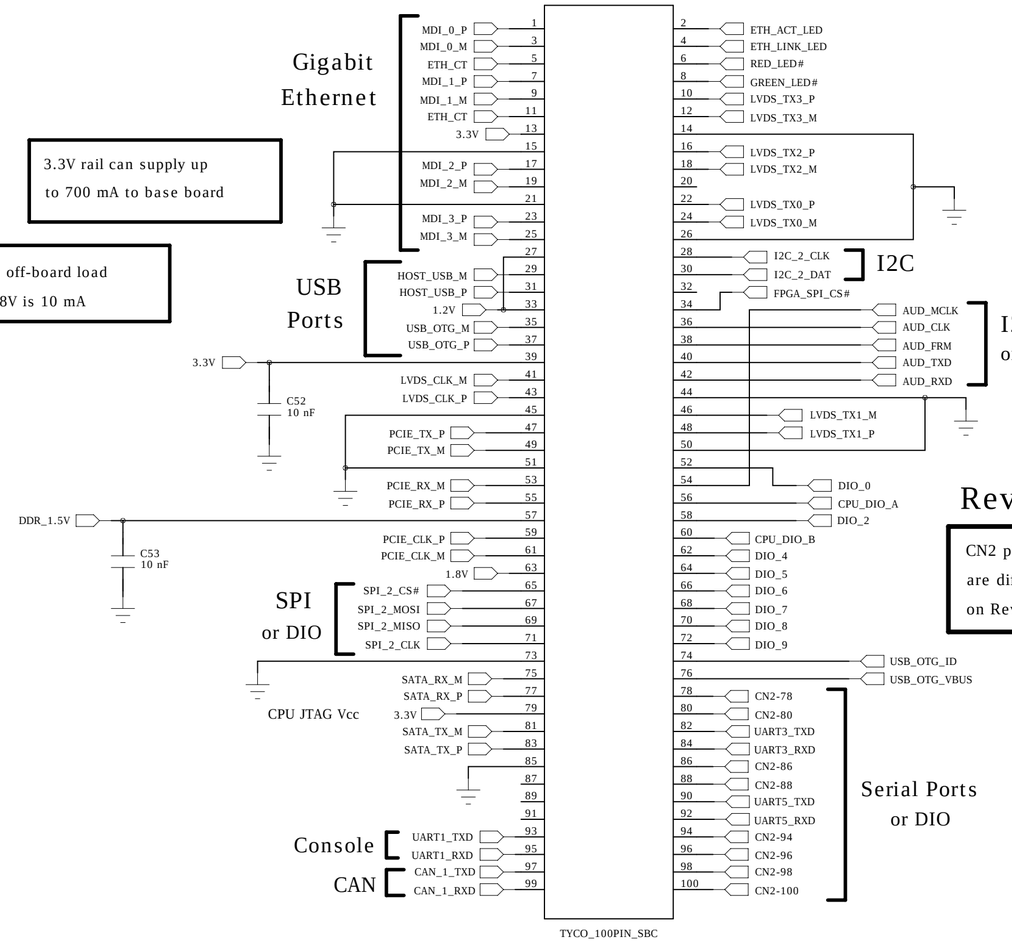
3.3V rail can supply up
to 700 mA to base board

Maximum off-board load
on AN_1.8V is 10 mA

Right

CN2

⚠ Pin 1 is the top left corner pin on the connector. All of the pins on the left are odd numbered. This may differ from the connector manufacture's datasheet.



Rev.C Change

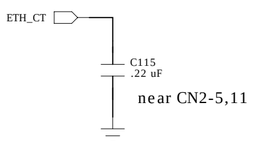
CN2 pins 56, 58, and 60
are different iMX6 balls
on Rev.C than on Rev.A

LVDS pairs are
length matched

PCIe Diff Pairs have
been Polarity swapped

SATA can NOT have
polarity swapped

SATA and PCIe Diff pairs do
NOT have to be length matched



Technologic Systems		Date Nov. 19, 2015
Title: TS-4900 Off-board Connectors		
Rev: D	Designer	Sheet 15 of 15