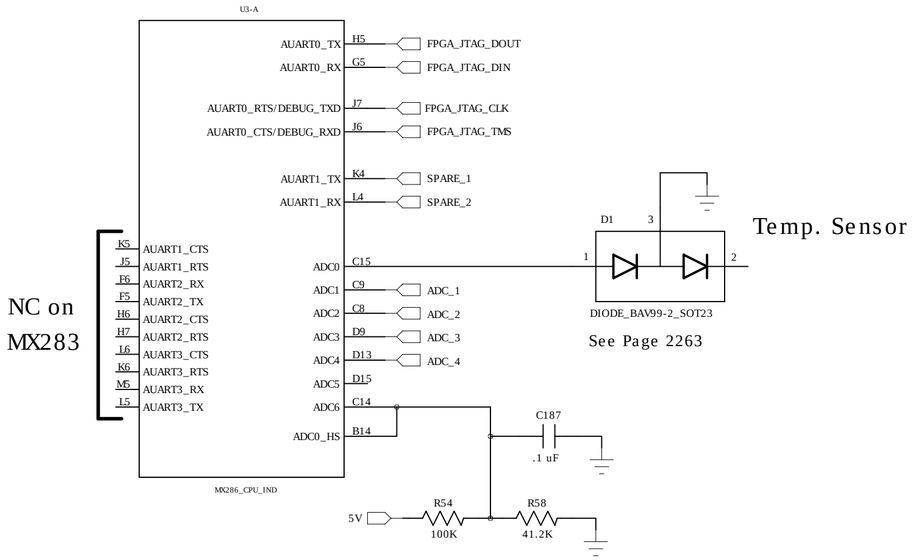
MX283/286 ARM9 CPU

UARTs, ADC



NC on MX283

Temp. Sensor

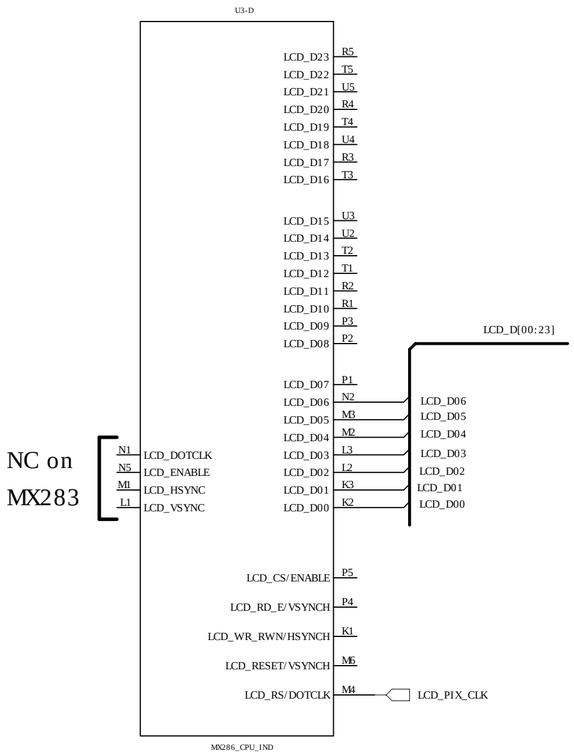
See Page 2263

Rev.A --> Rev.B

Connected CAN bus to FPGA

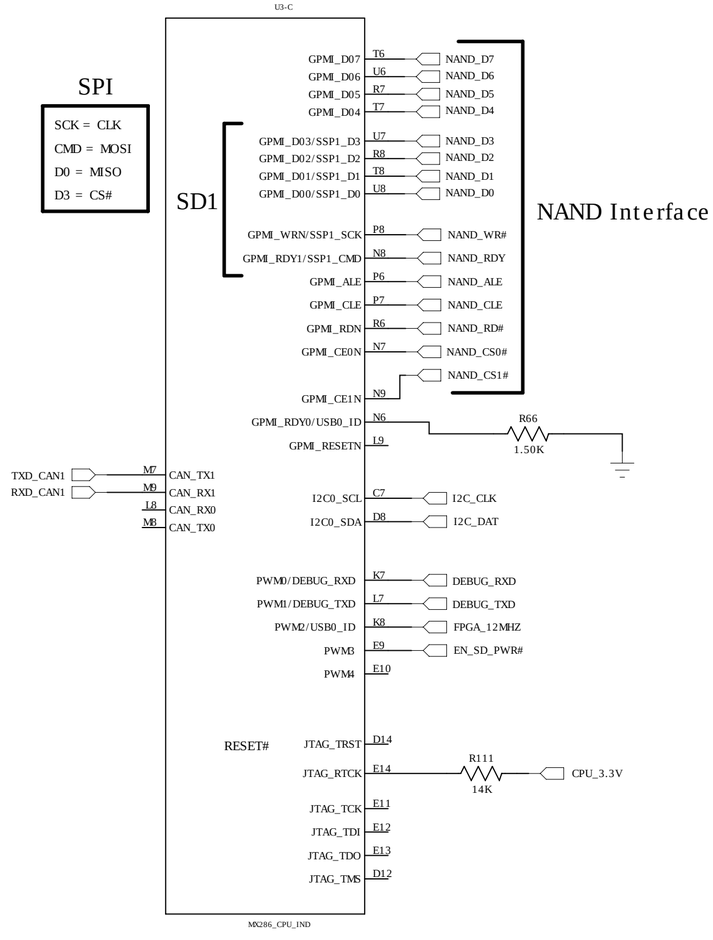
CPU changed to MX286

LCD



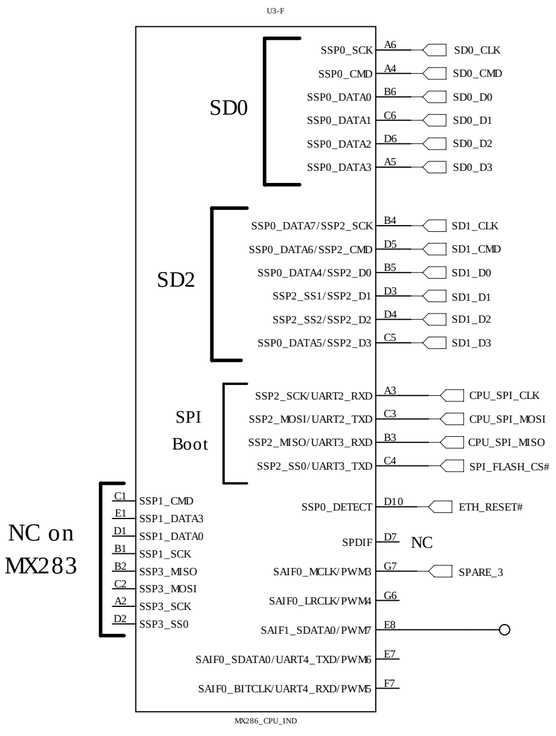
NC on MX283

NAND, PWM
JTAG, I2C



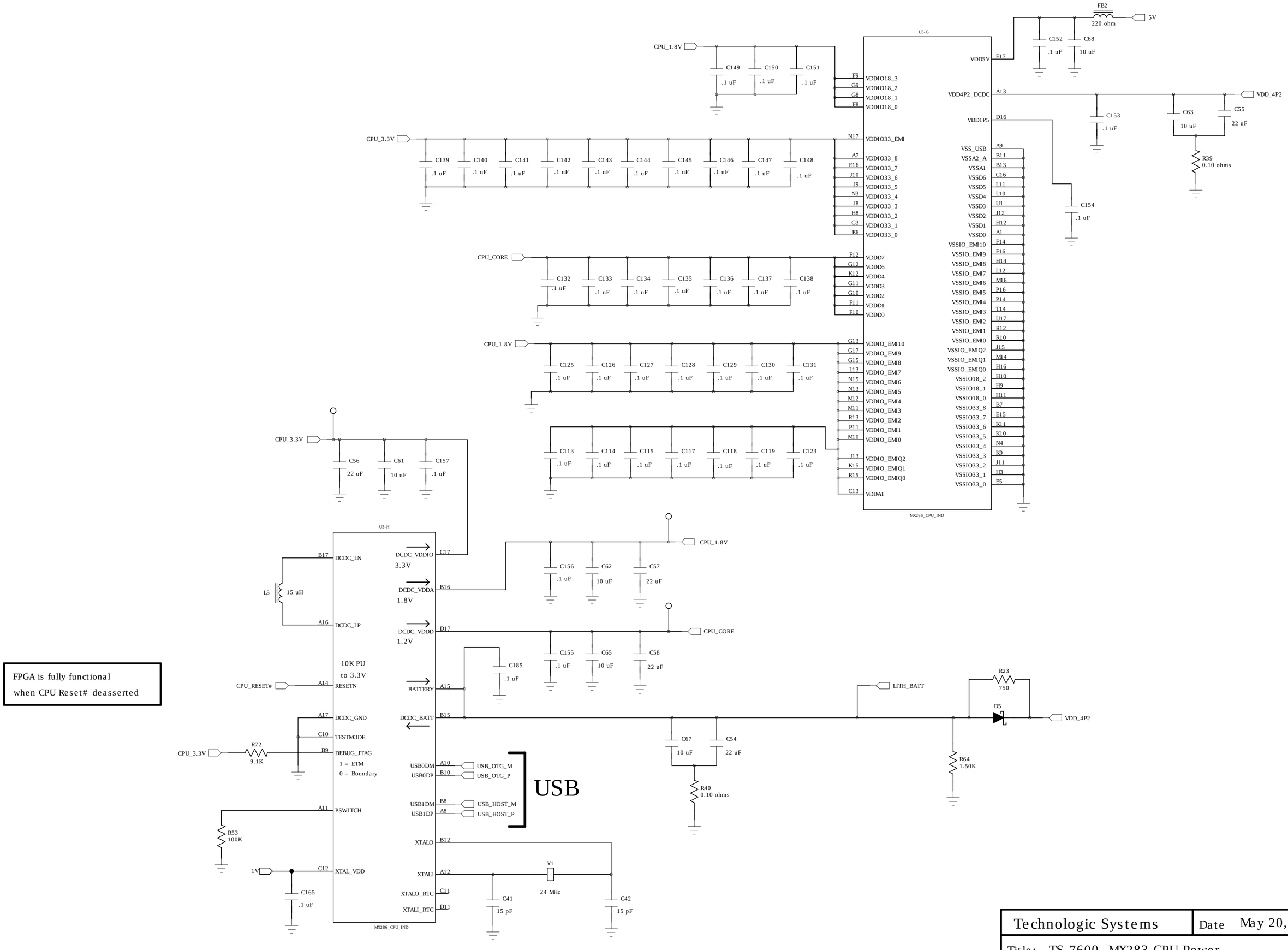
NAND Interface

Audio
SD Card
SPI Boot



NC on MX283

Technologic Systems	Date May 20, 2014	
Title: TS-7600 MX283 CPU		
Rev: B	Designer	Sheet 1 of 9

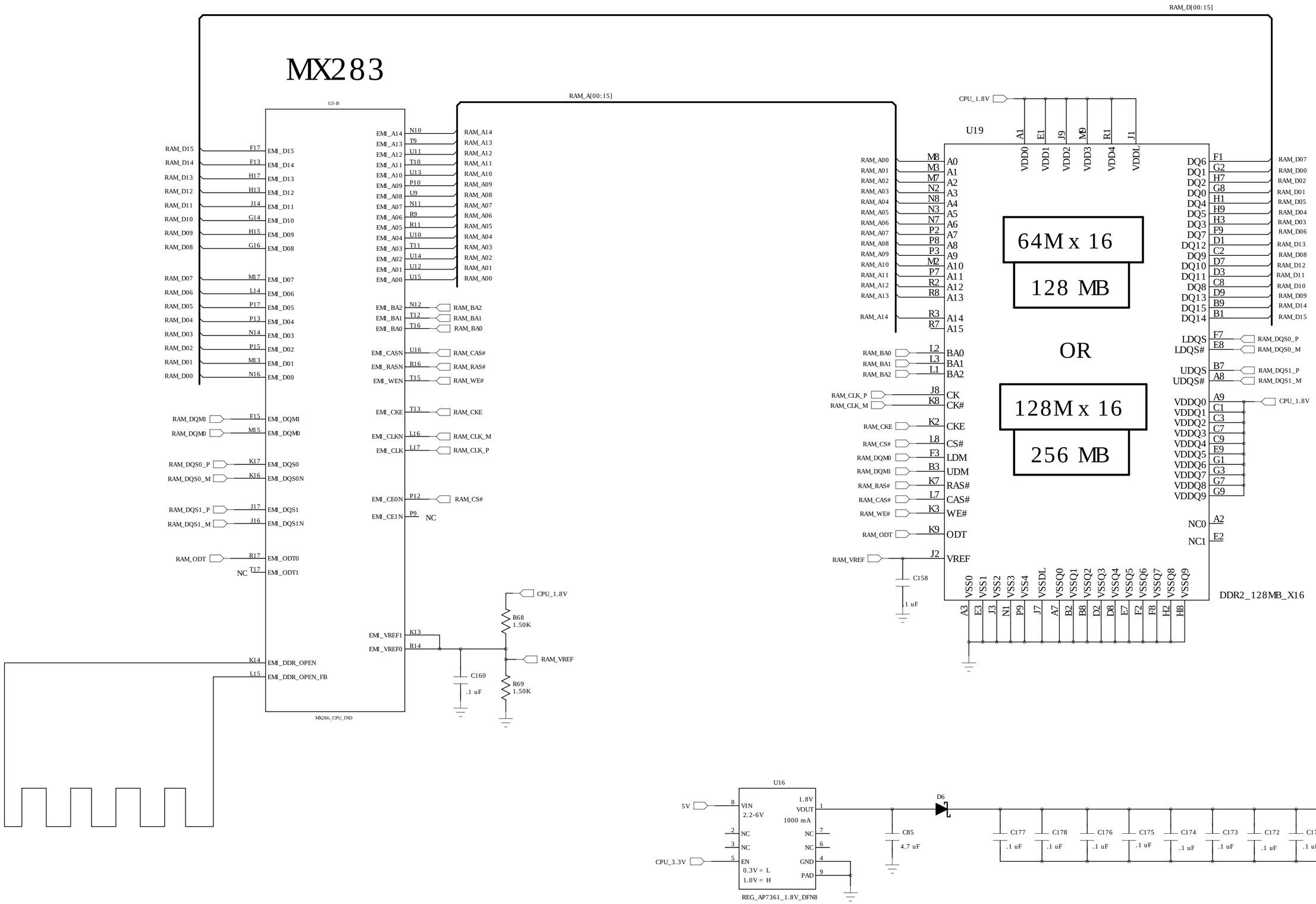


FPGA is fully functional
when CPU Reset# deasserted

PSWITCH can be driven to 3.3V if a series 10K res is used

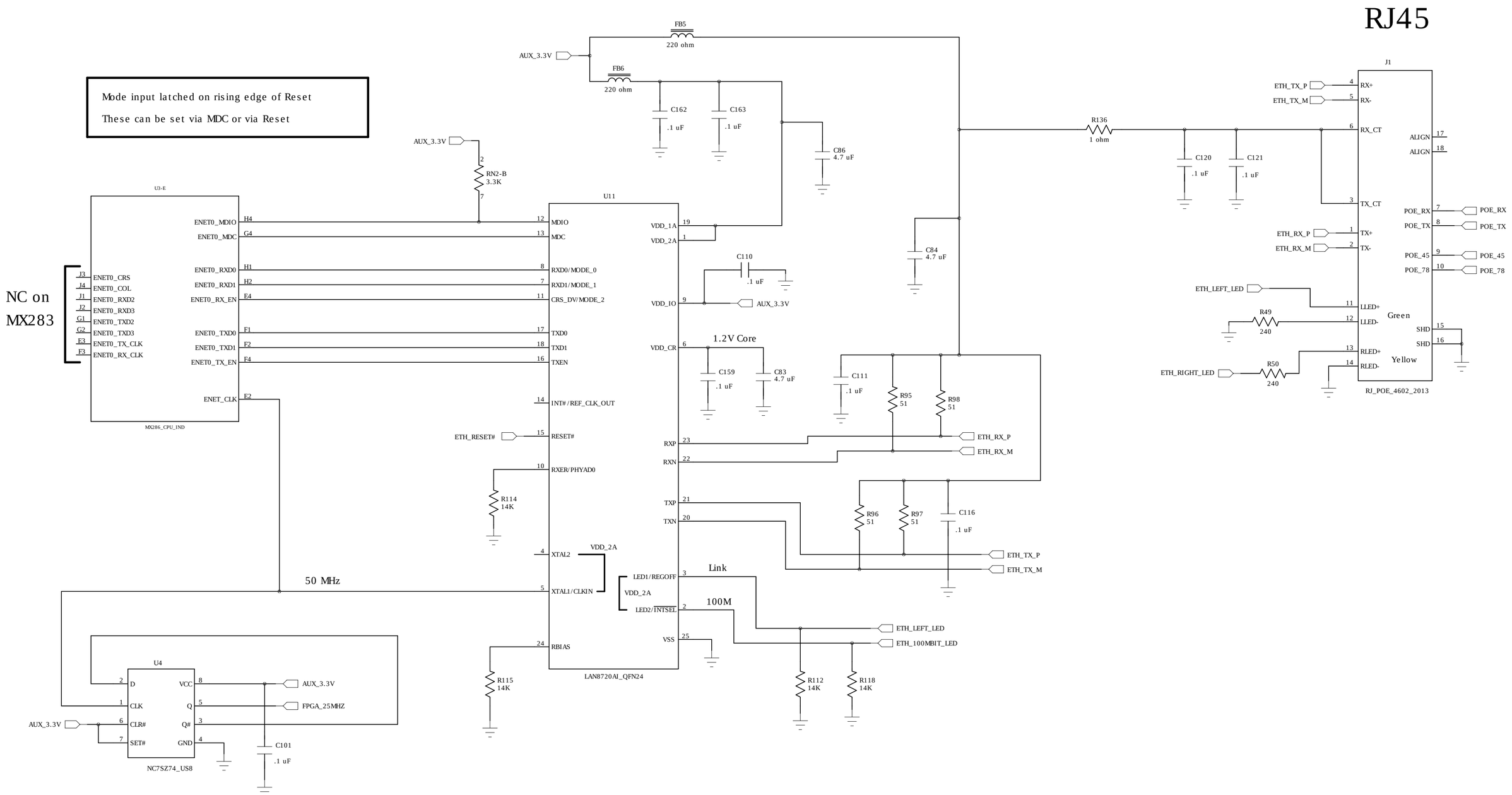
Technologic Systems	Date May 20, 2014	
Title: TS-7600 MX283 CPU Power		
Rev: B	Designer	Sheet 2 of 9

DDR2 SDRAM (128 or 256 MByte)



Technologic Systems		Date May 20, 2014
Title: TS-7600 DDR2 RAM		
Rev: B	Designer	Sheet 3 of 9

10/100 Ethernet

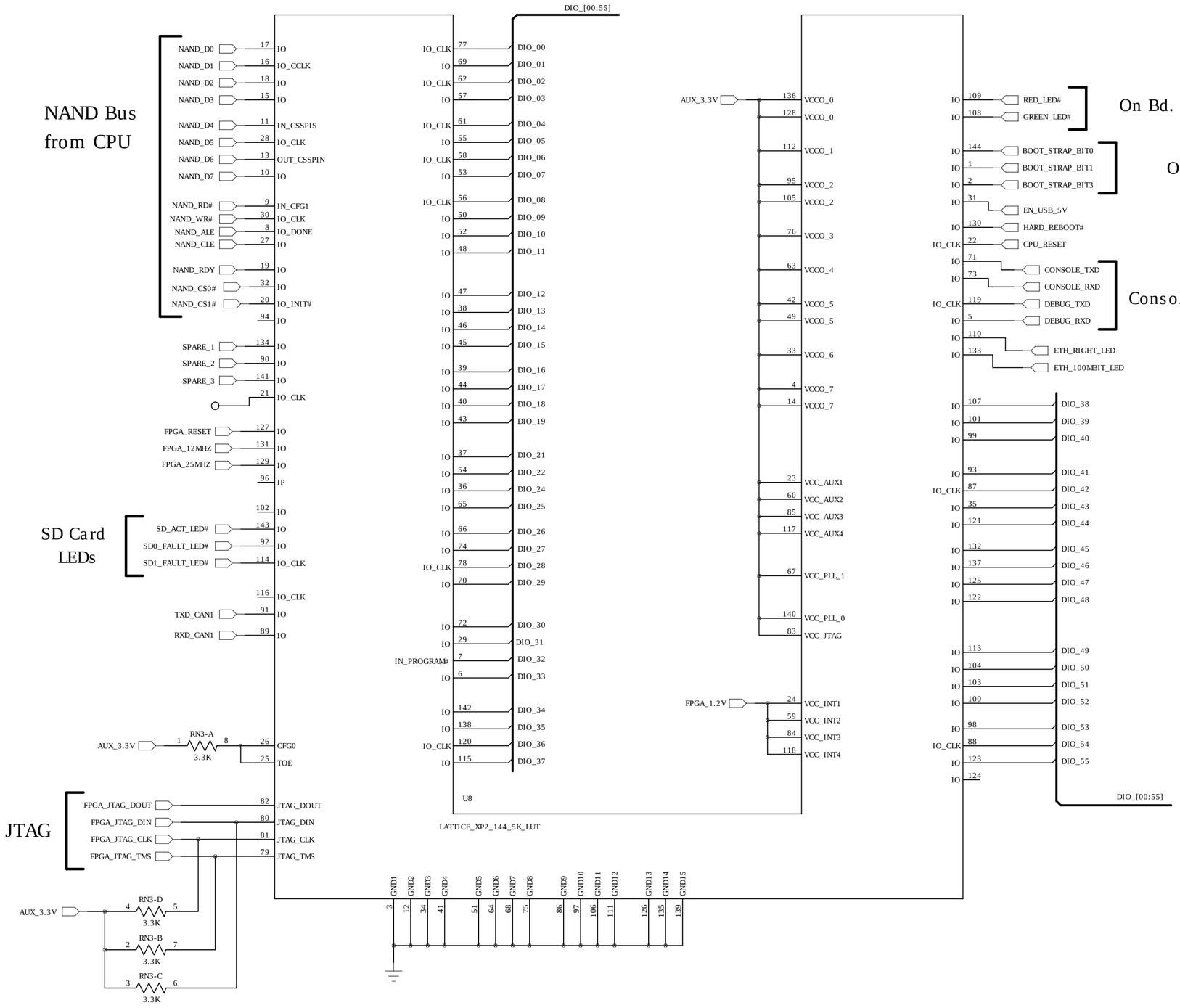


Auto MDIX is supported and

Polarity Correction supported

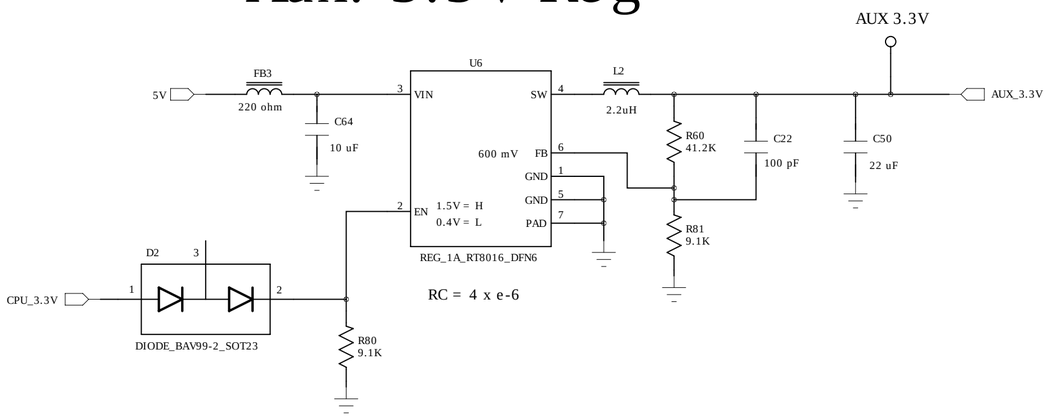
Technologic Systems		Date May 20, 2014
Title: TS-7600 Ethernet Port		
Rev: B	Designer	Sheet 4 of 9

FPGA with 5K LUTs

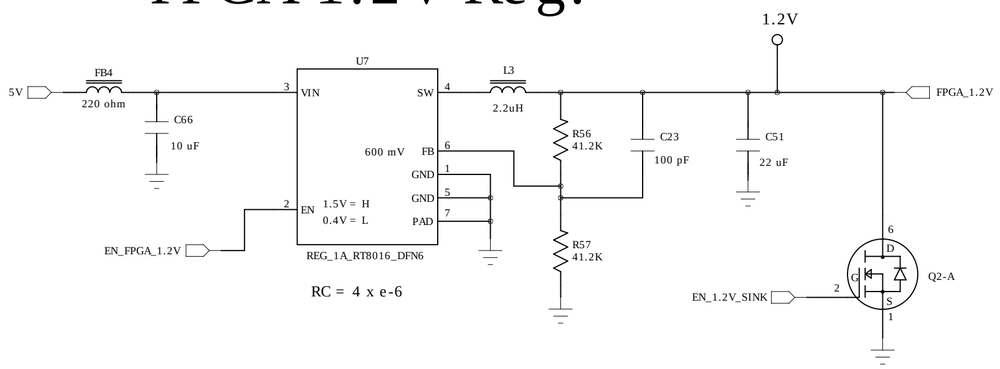


Technologic Systems		Date May 20, 2014
Title: TS-7600 FPGA		
Rev: B	Designer	Sheet 5 of 9

Aux. 3.3V Reg

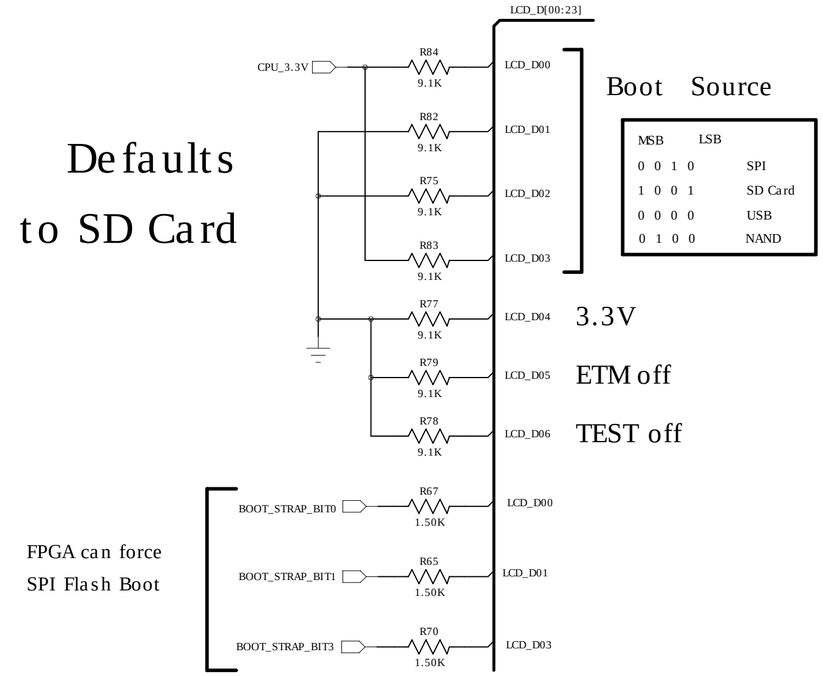


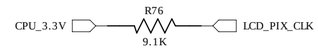
FPGA 1.2V Reg.



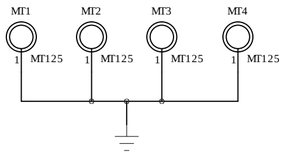
Boot Strap Bias Res.

Defaults to SD Card





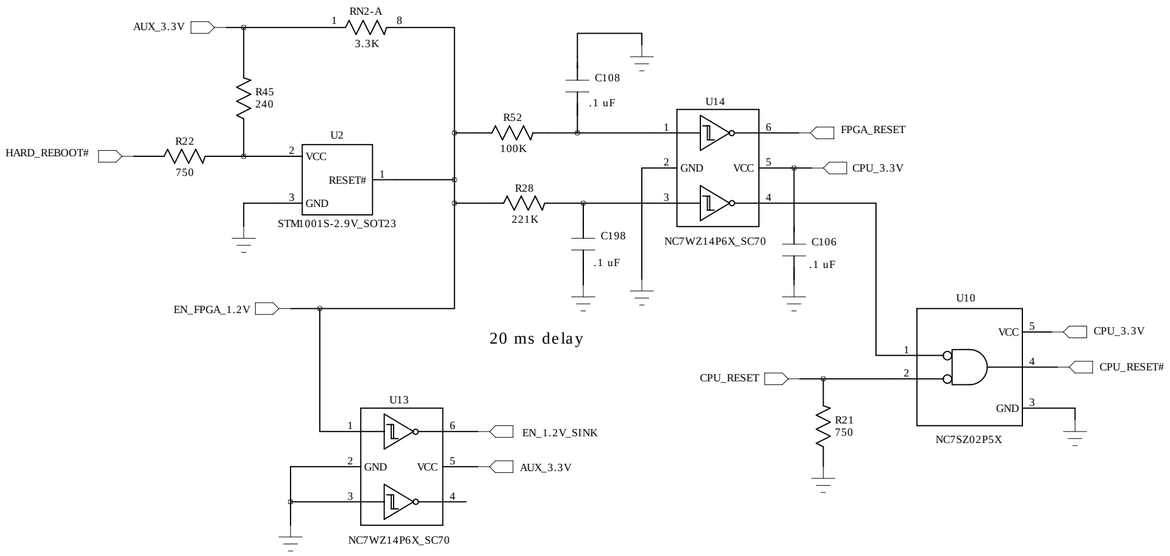
GND Test Point



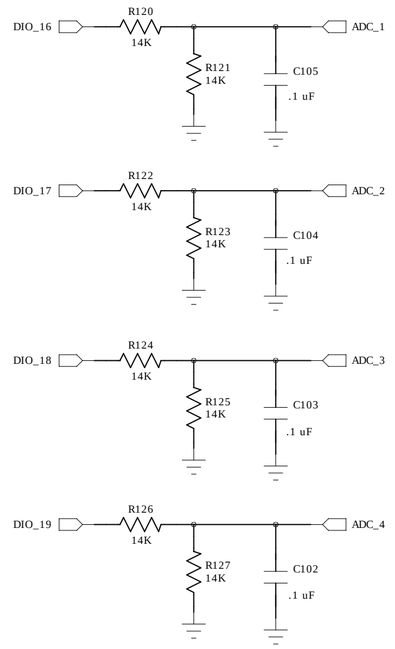
Technologic Systems	Date May 20, 2014	
Title: TS-7600 Power Reg. and Boot Straps		
Rev: B	Designer	Sheet 6 of 9

RTC and Reset Sequencer

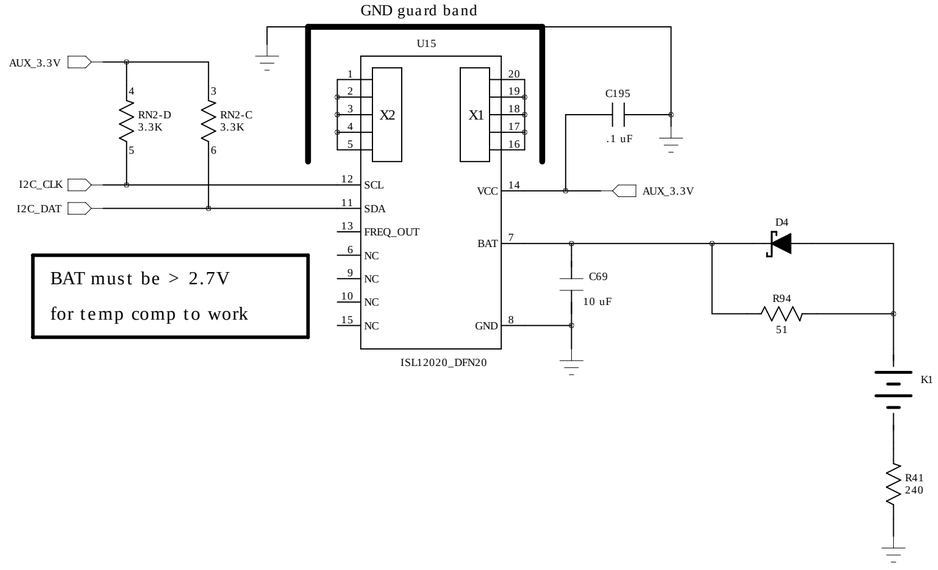
Reset Sequencer



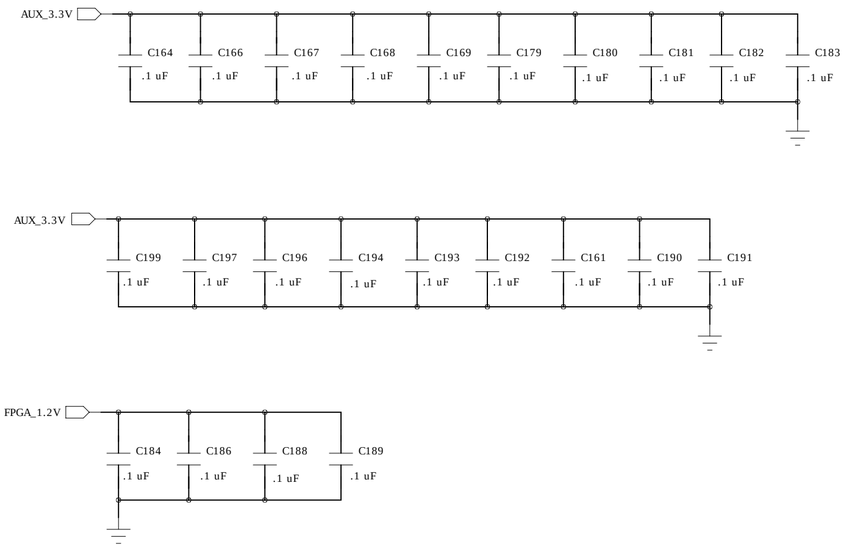
Analog Inputs



RTC and Temp. Sensor

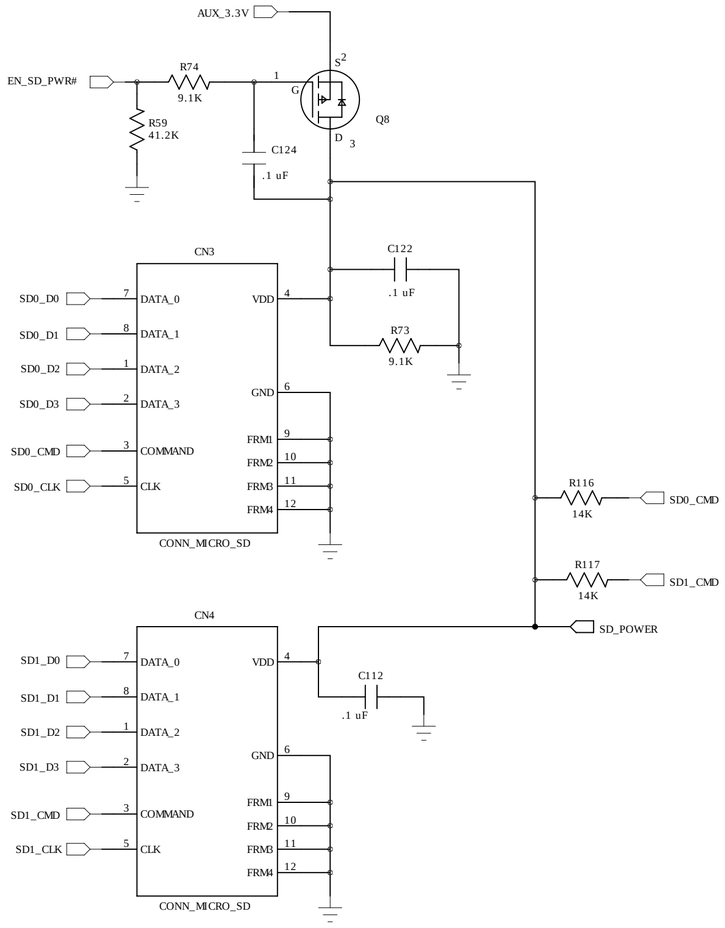


FPGA Bypass Caps

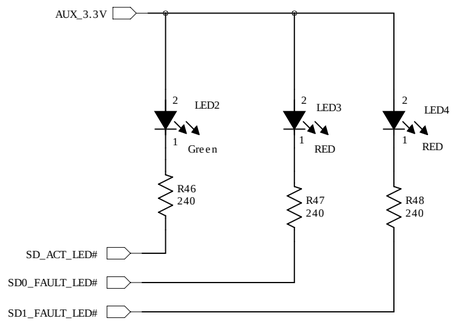


Technologic Systems	Date May 20, 2014	
Title: TS-7600 Boot Flash, RTC, Reset		
Rev: B	Designer	Sheet 7 of 9

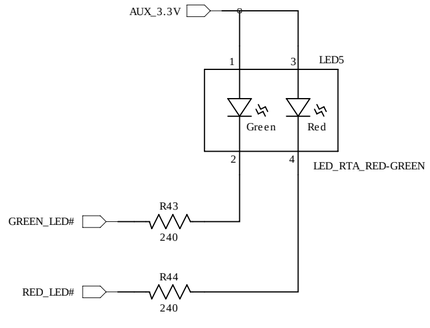
Micro SD Card Sockets



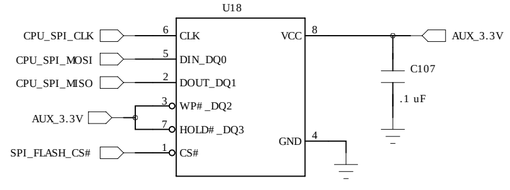
SD LEDs



Red/Green LEDs



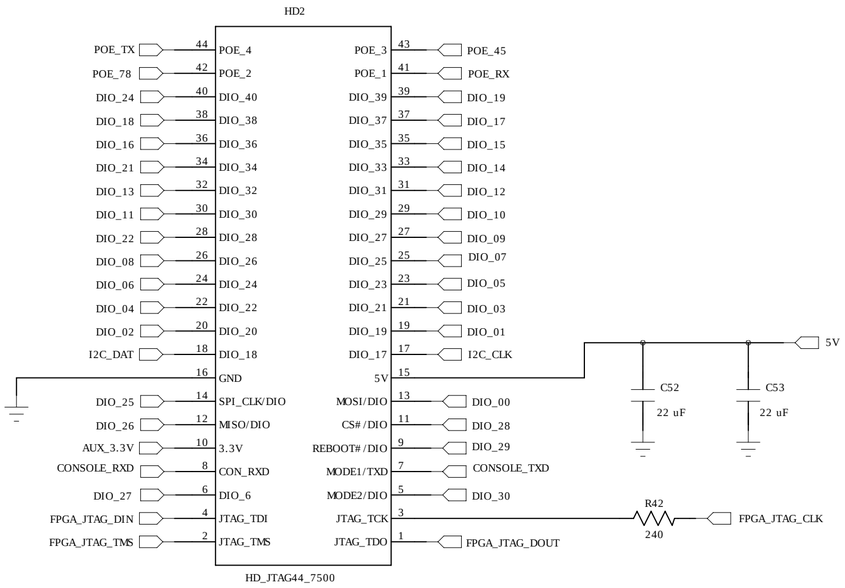
SPI Boot Flash



64 bytes of OTP

Technologic Systems		Date May 20, 2014
Title: TS-7600 SD Card		
Rev: B	Designer	Sheet 8 of 9

44-Pin DIO Header



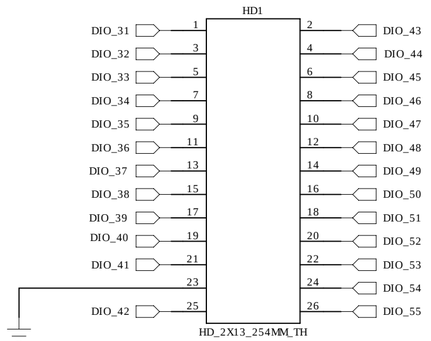
MODE1 and MODE2 states are latched when CPU_RESET# is deasserted

Logic "0" on MODE2 signal forces Boot from SD card

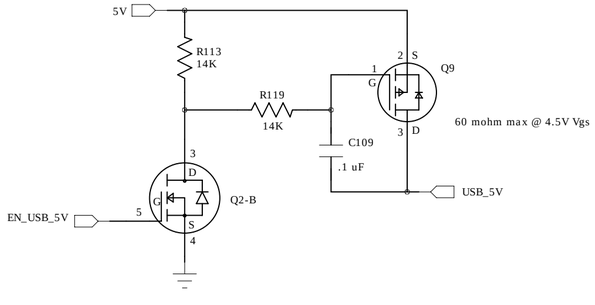
MODE1 and MODE2 have 4.7K resistor pull-ups on TS-7500

Logic "0" on MODE1 forces Console onto the TXD and RXD lines

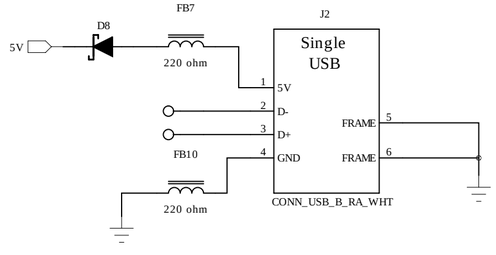
26-Pin DIO Header



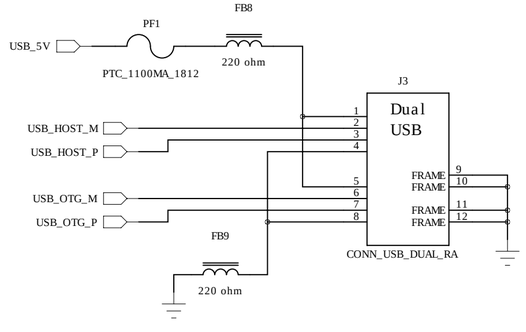
USB 5V



USB Device Port



USB Host Ports



Technologic Systems		Date May 20, 2014
Title: TS-7600 44-pin DIO and USB		
Rev: B	Designer	Sheet 9 of 9