TS-7800

Changes from Rev. E to G

Fixed Left Ethernet LED (reversed polarity)

Changed to new Full-size SD card socket Due to EOL on old socket

Added TVS and res on DIO Header for keypad

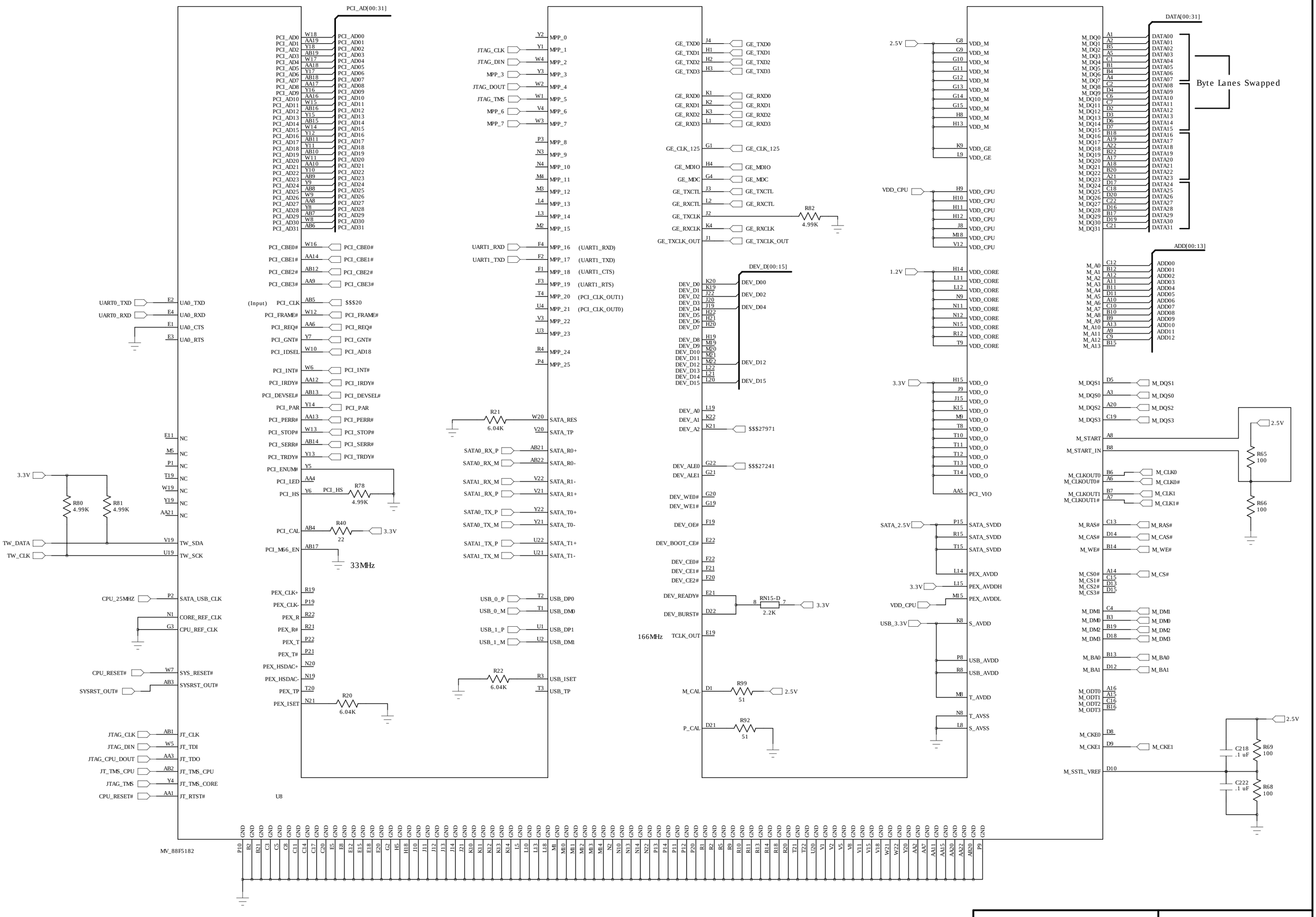
Added Console TVS on COM3

Improve clearance for bottom parts

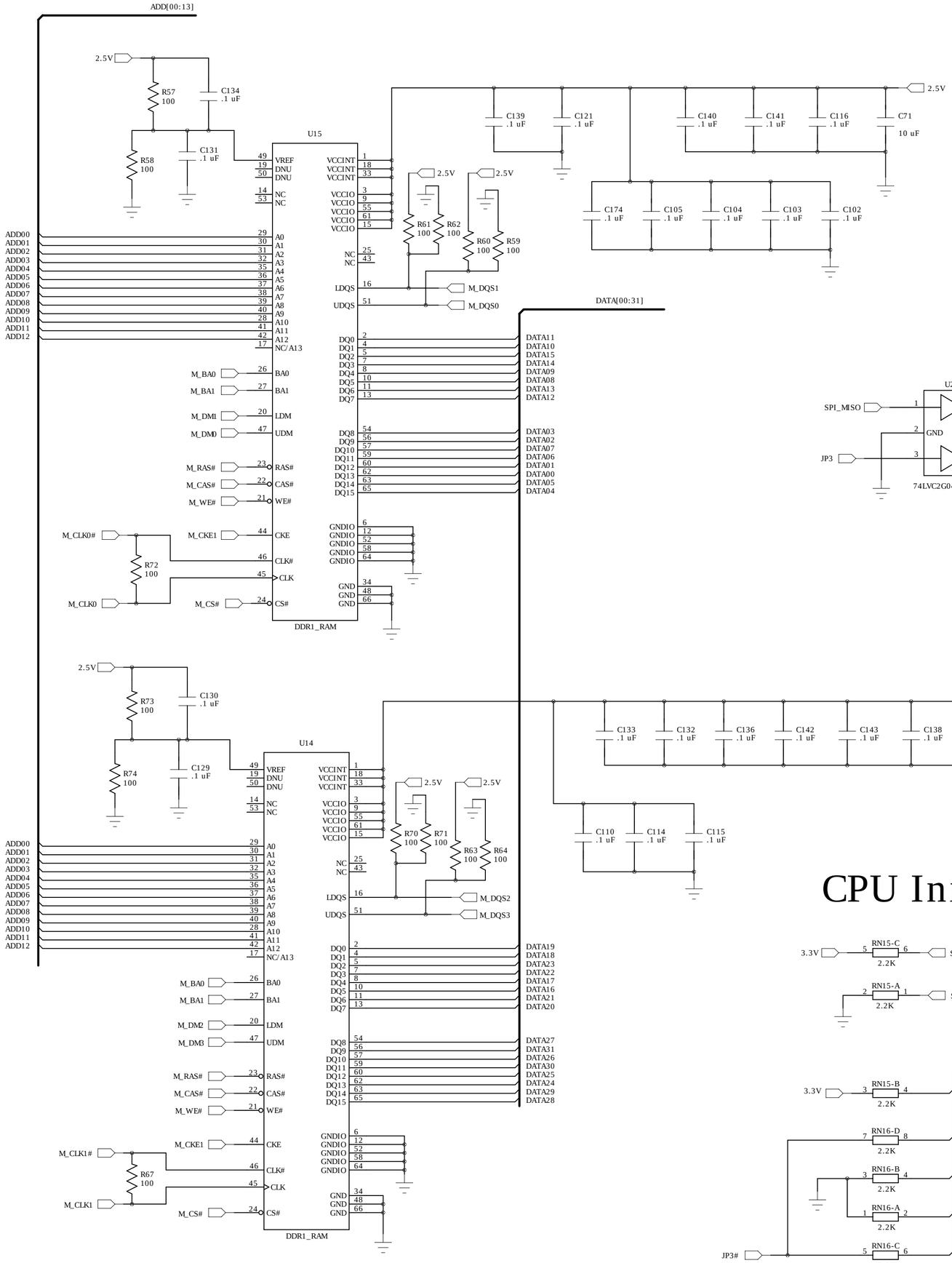
Added R15 (0 Ohms) to connect Frame to GND

Improved board design with more by pass caps

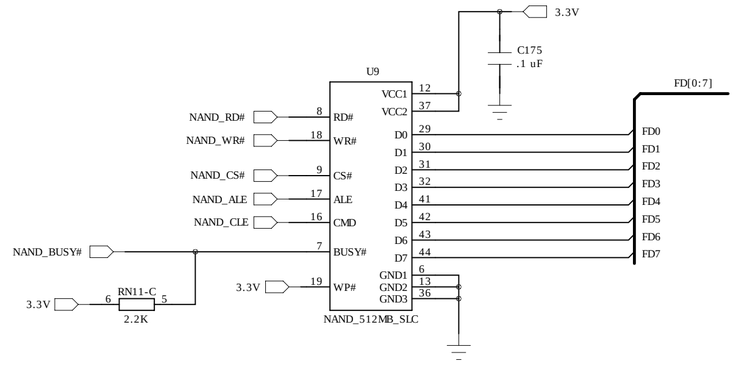
Technologic Systems		Date July 23, 2015
Title: TS-7800 Documentation		
Rev: G	Designer	Sheet 1 of 12


PCI_AD[00:31]
DATA[00:31]
Byte Lanes Swapped
ADD[00:13]
DEV_D[00:15]
MV_88F5182
U8
Start_Burst length = Ave of 4 data lanes + CLK
Technologic Systems
Date July 23, 2015
Title: TS-7800 Marvell 88F5182 CPU
Rev: G
Designer RLM
Sheet 2 of 12

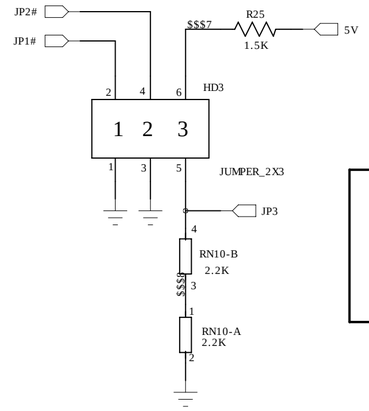
DDR1 SDRAM



NAND Flash



Jumpers

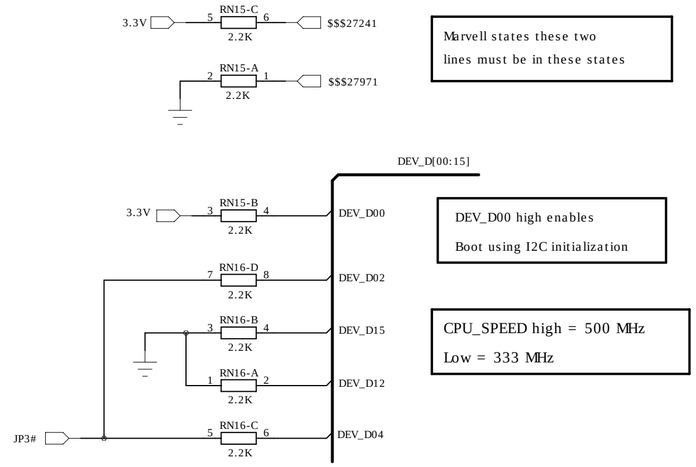


JP1 = Fast Boot to NAND Flash

JP2 = Enable console on COM1

JP3 = CPU Speed is 333 MHz

CPU Initialization

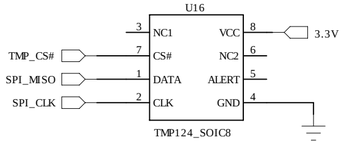


Marvell states these two lines must be in these states

DEV_D00 high enables Boot using I2C initialization

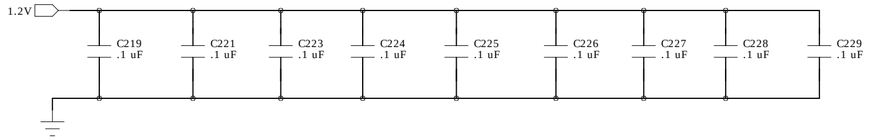
CPU_SPEED high = 500 MHz
Low = 333 MHz

Temp Sensor

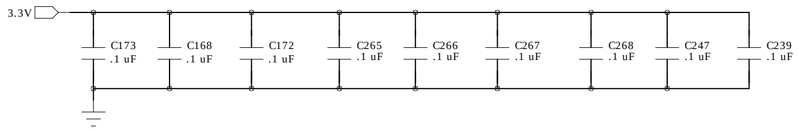


Technologic Systems	Date July 23, 2015	
Title: TS-7800 DDR RAM Flash		
Rev: G	Designer	Sheet 3 of 12

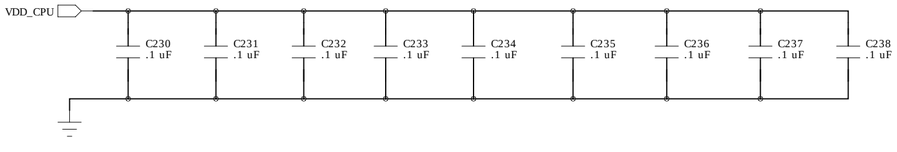
Near CPU



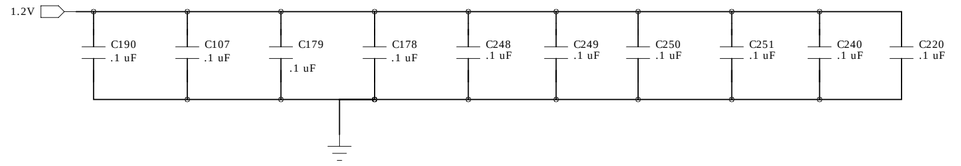
Near FPGA



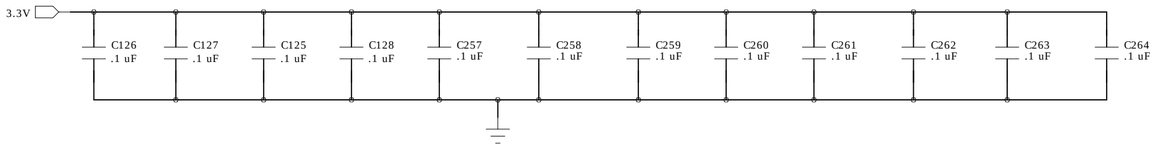
Near CPU



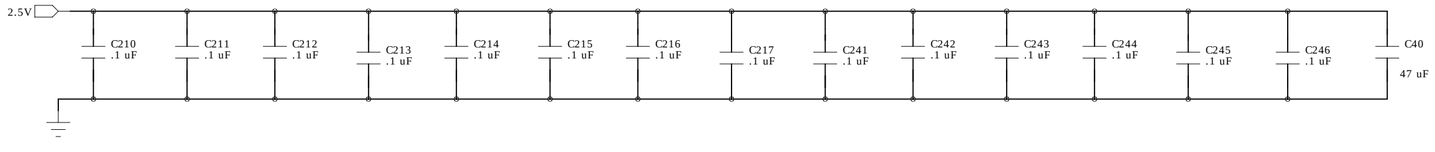
Near FPGA



Near CPU



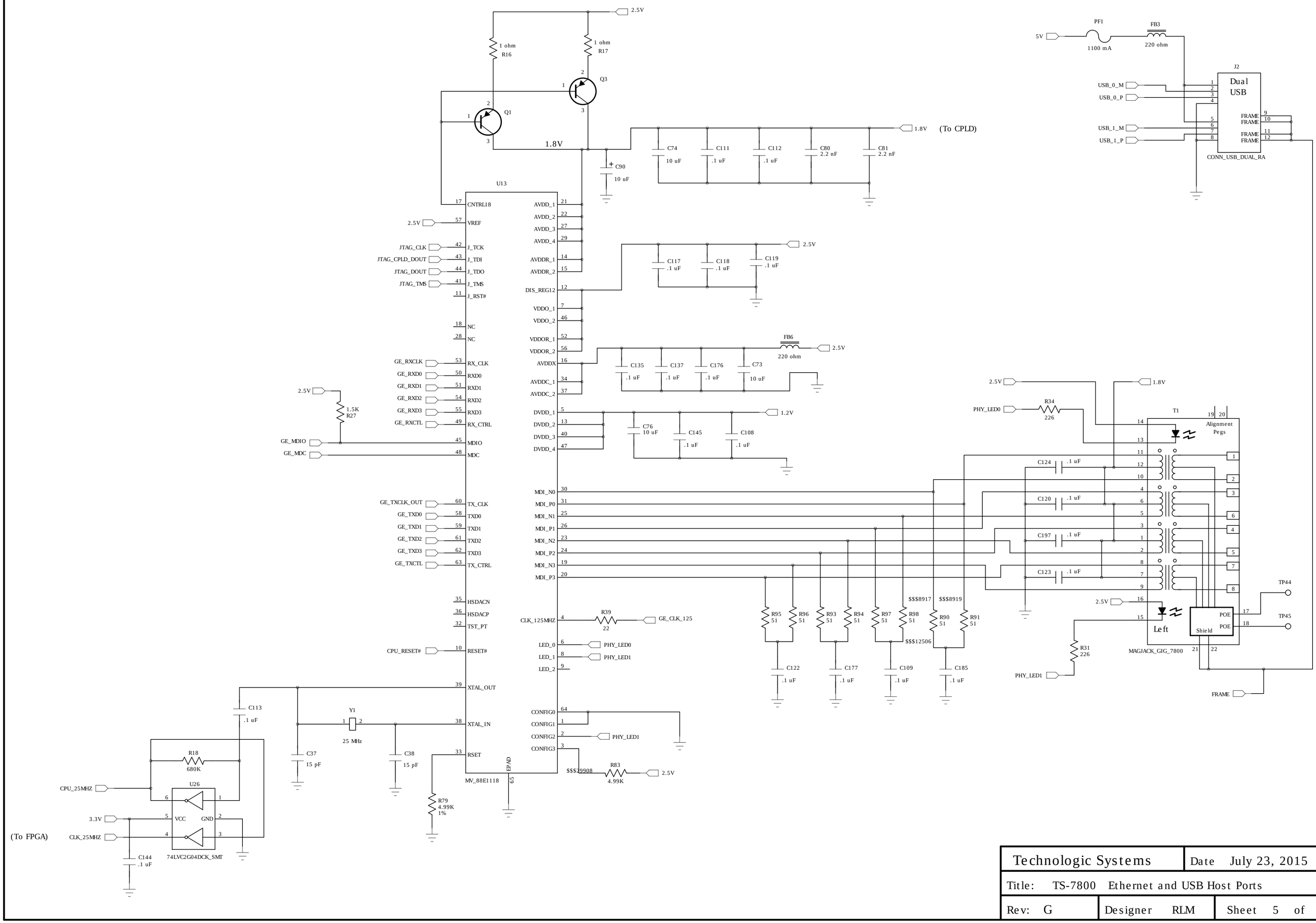
Near CPU



Technologic Systems		Date July 23, 2015
Title: TS-7800 Bypass Caps		
Rev: G	Designer	Sheet 4 of 12

10/100/1000 Ethernet

USB Ports



Technologic Systems	Date July 23, 2015	
Title: TS-7800 Ethernet and USB Host Ports		
Rev: G	Designer RLM	Sheet 5 of 12

5V Tolerant CPLD

SPI Serial Flash

U10 — LATTICE_ECP2_256

U19 — MACH4064ZC

U20 — FLASH_SPI_4MBIT_SOIC8

ISA_DAT[00:15]
ISA_A[01:31]
ISA_C[01:10]
FD[0:7]
PCI_AD[00:31]
ISA_B[02:30]
ISA_D[01:17]
PLD_D[0:5]
DIO_[01:15]
LCD_[03:14]

All PBxx pins have PCI clamp diodes
These are all in Bank4 and Bank5

Enable Resistor Pull-ups
on all pins (Global option)

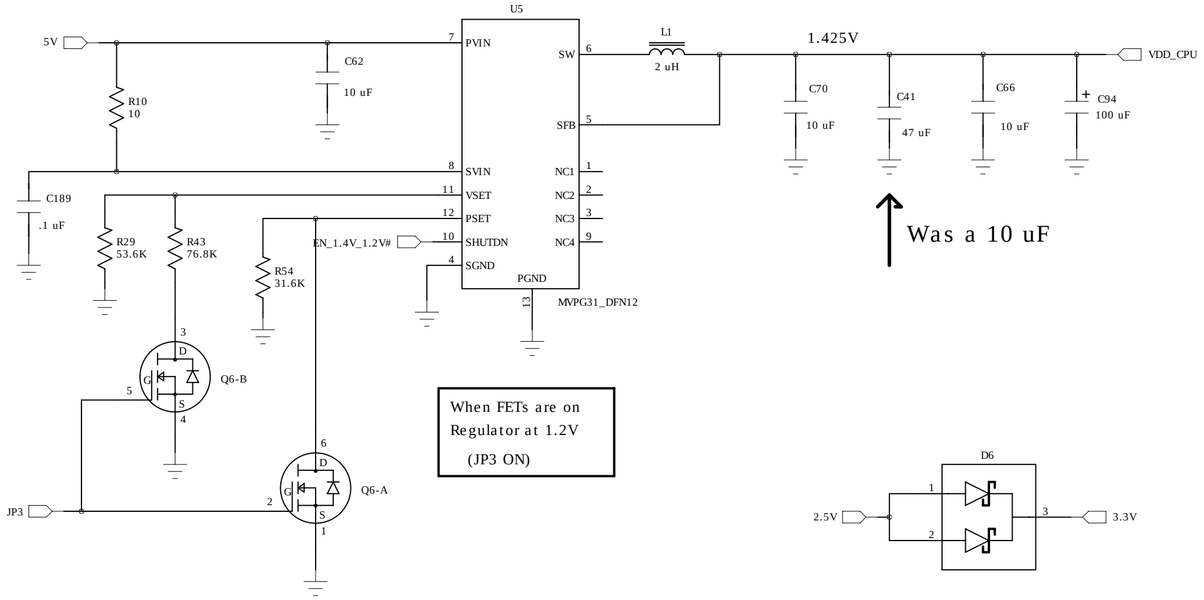
SPI Fast Mode is selected
when pin M16 is biased low

Config_CLK is output in SPI Mode
and is an input in Serial Config Mode
SPI Mode requires resistor pull-down

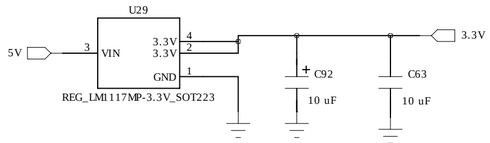
Pin K11 is Data Input for Ser. Config
It is the Serial Flash CS# for SPI Mode

Technologic Systems	Date July 23, 2015	
Title: TS-7800 FPGA and PLD		
Rev: G	Designer	Sheet 6 of 12

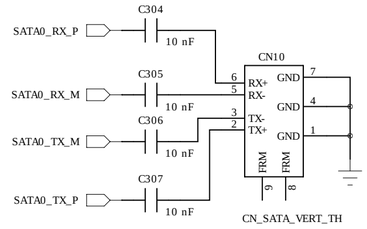
1.2V or 1.42V Power Supply

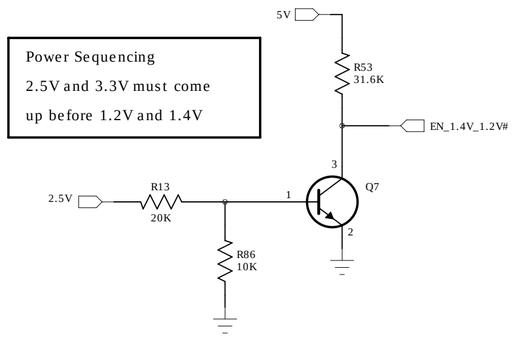


3.3V Regulator



SATA 0

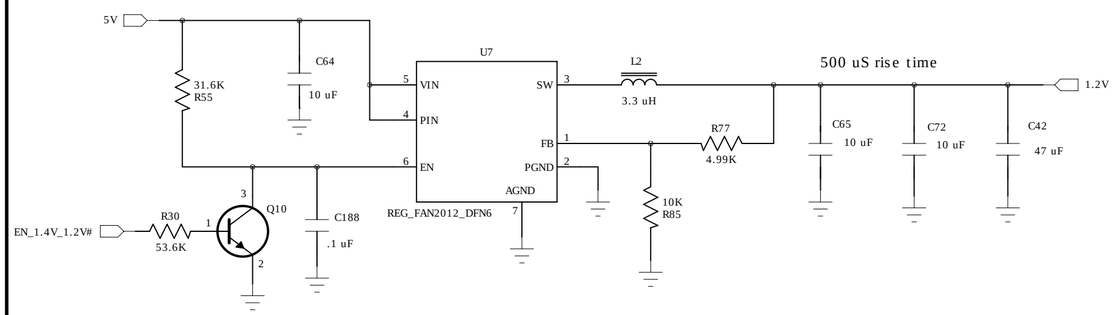




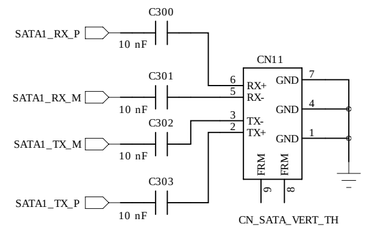
Power Sequencing
2.5V and 3.3V must come
up before 1.2V and 1.4V

1.2V Power Supply

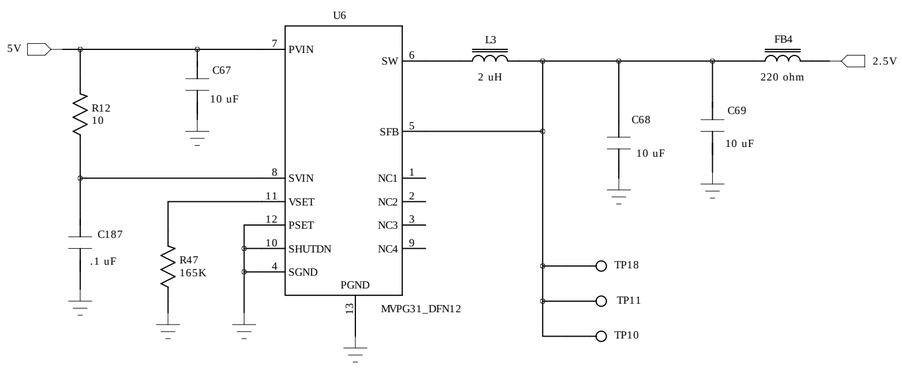
up to 1500 mA



SATA 1



2.5V Power Supply



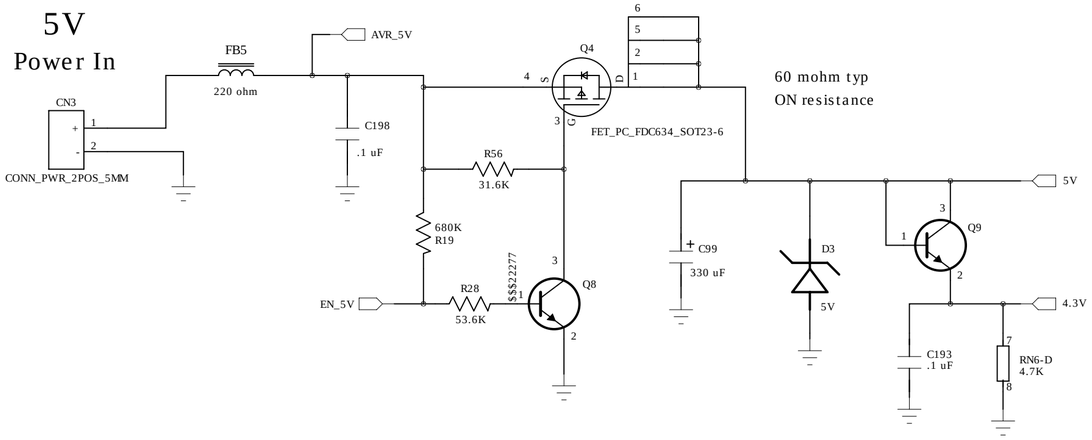
SATA can NOT have
polarity swapped

SATA and PCIe Diff pairs do
NOT have to be length matched

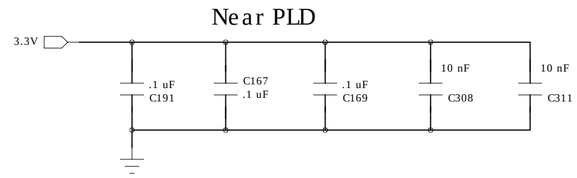
Technologic Systems	Date July 23, 2015	
Title: TS-7800 Power		
Rev: G	Designer	Sheet 7 of 12

5V Switch

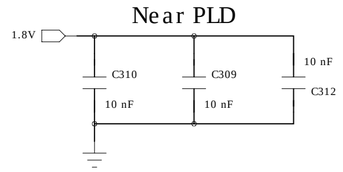
5V
Power In

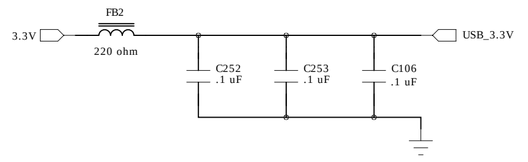


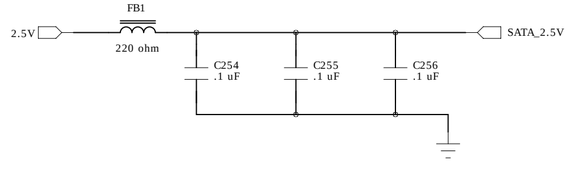
Near PLD



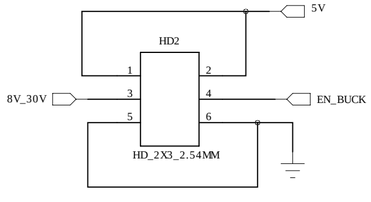
Near PLD





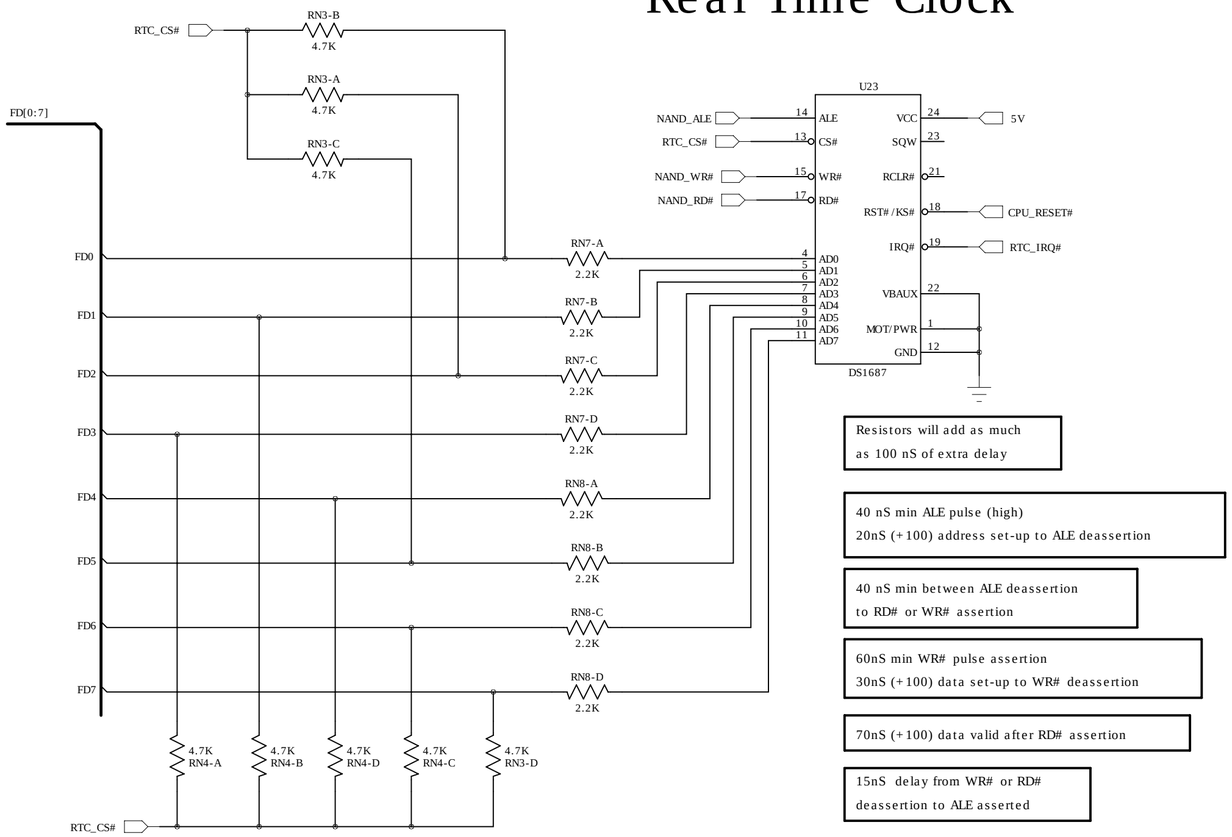


Interface to Buck Reg.



Technologic Systems	Date July 23, 2015	
Title: TS-7800 Power		
Rev: G	Designer	Sheet 8 of 12

Real Time Clock



Resistors will add as much as 100 nS of extra delay

40 nS min ALE pulse (high)
20nS (+100) address set-up to ALE deassertion

40 nS min between ALE deassertion to RD# or WR# assertion

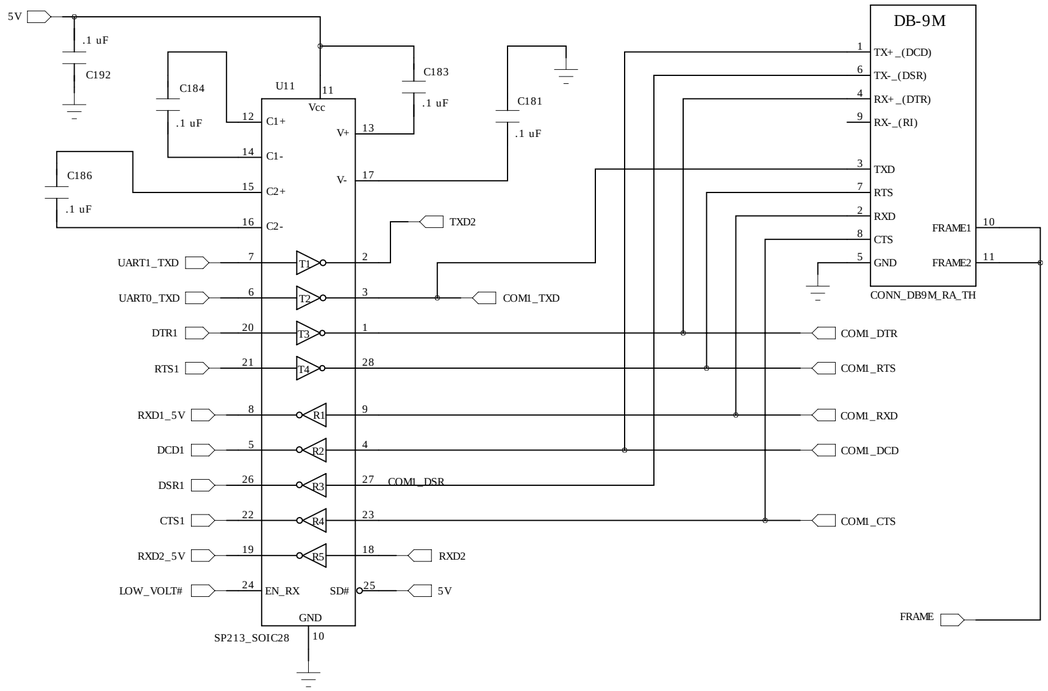
60nS min WR# pulse assertion
30nS (+100) data set-up to WR# deassertion

70nS (+100) data valid after RD# assertion

15nS delay from WR# or RD# deassertion to ALE asserted

COM1

RS-232 Transceiver

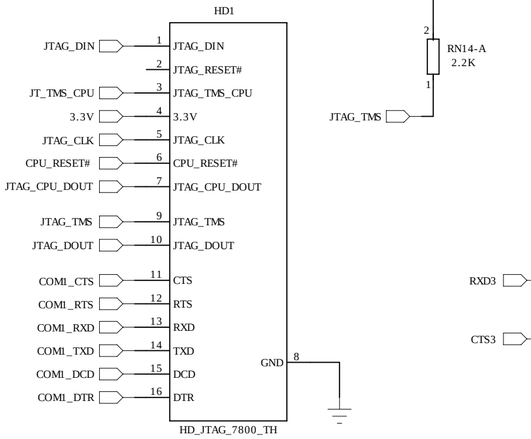


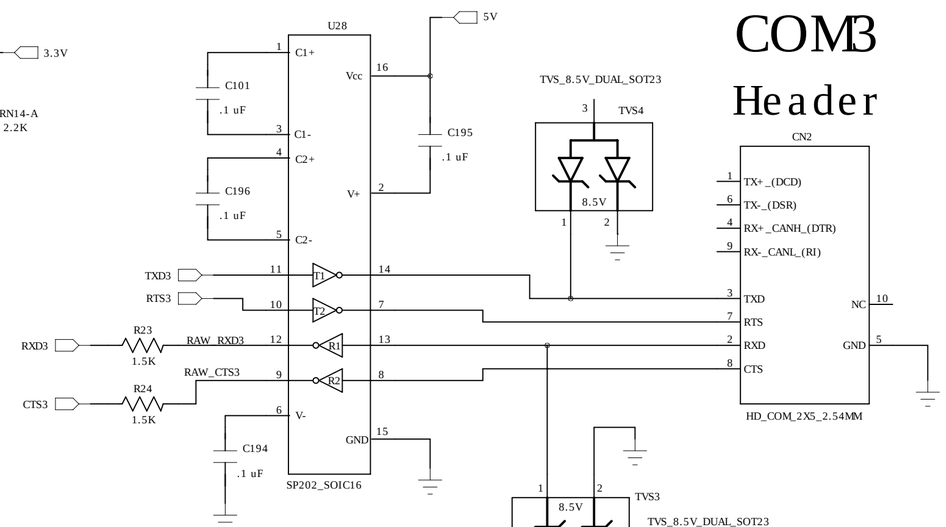
COM1

DB9M

JTAG

Header

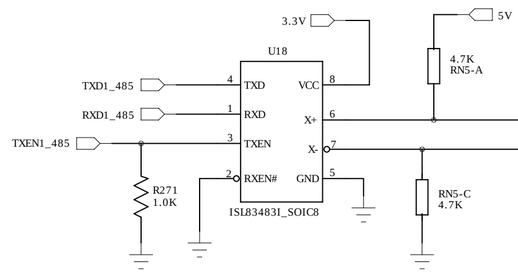


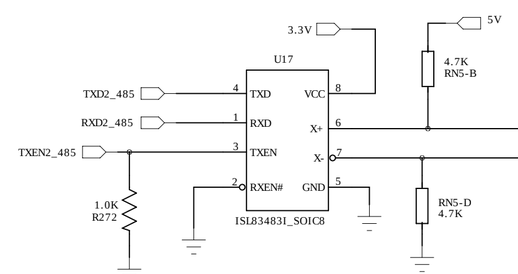


COM3

Header

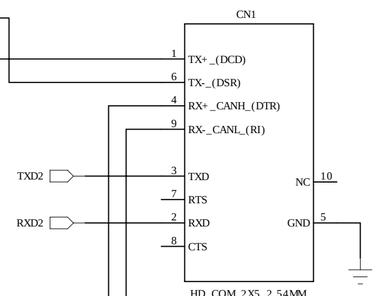
RS-485 Drivers



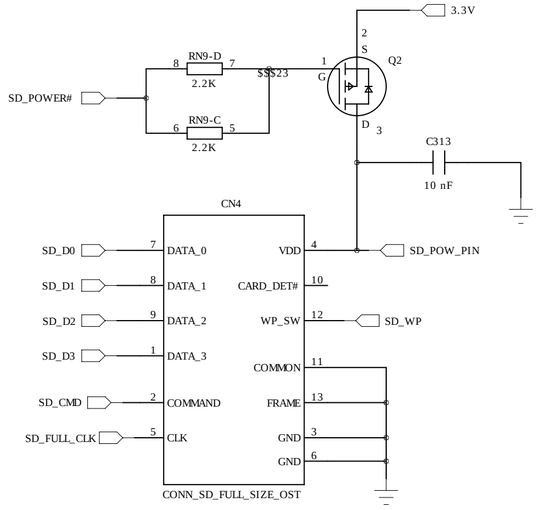


COM2

Header



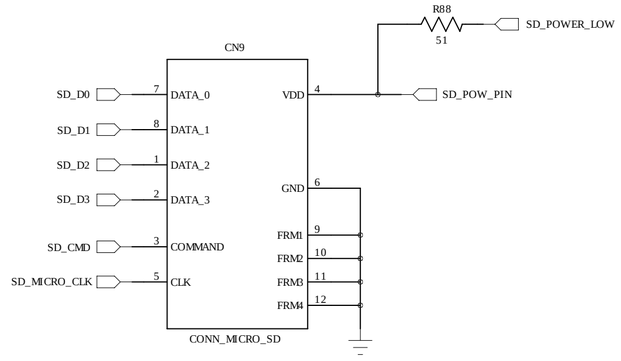
Technologic Systems	Date July 23, 2015	
Title: TS-7800 RTC, COM Ports, JTAG Header		
Rev: G	Designer	Sheet 9 of 12



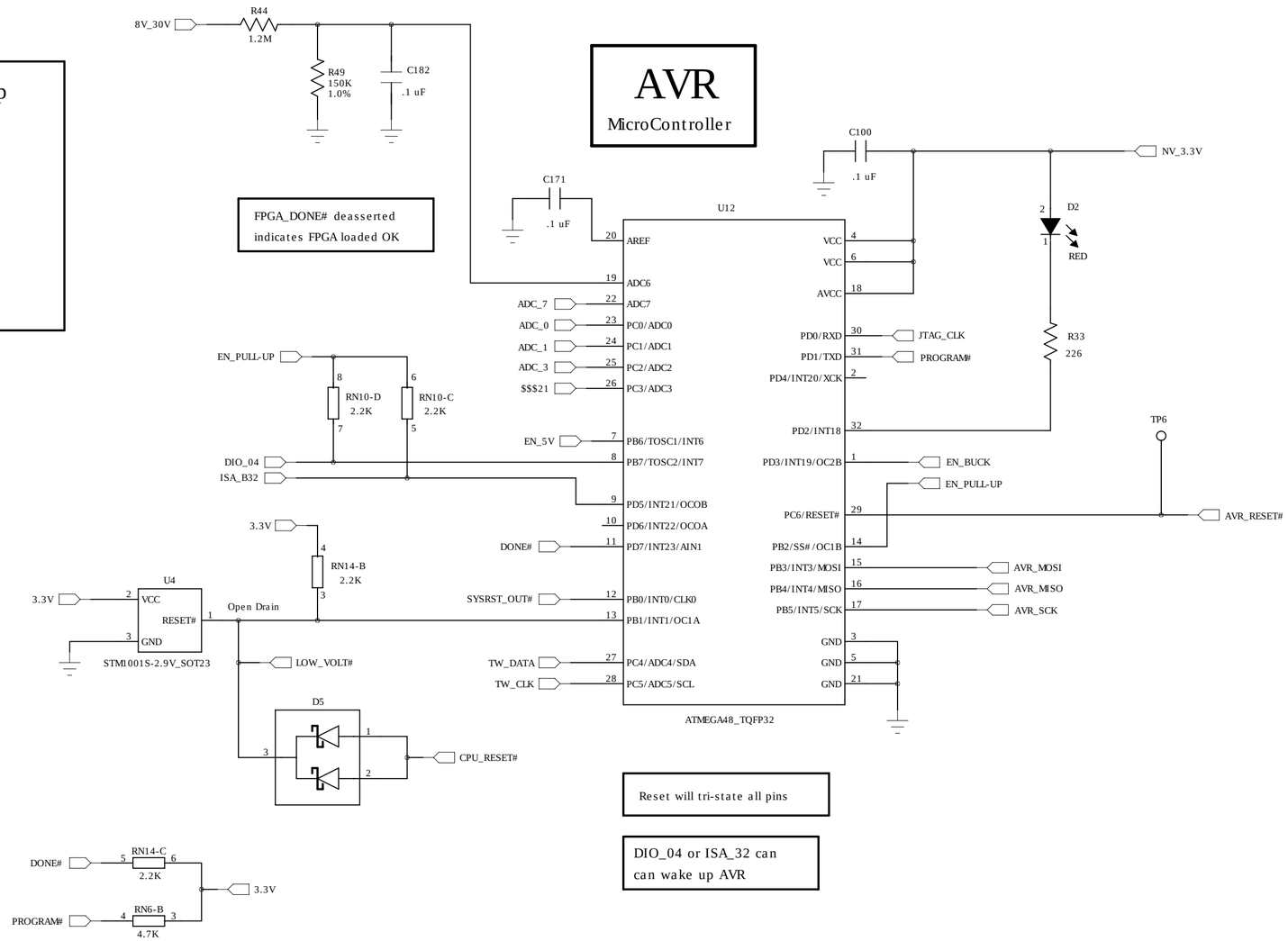
Must enable pull-up resistors for these pins:

- SD card D0-D3
- SD Power#
- SD card WP

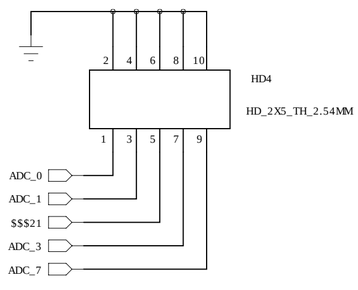
Full-Size SD Card Socket



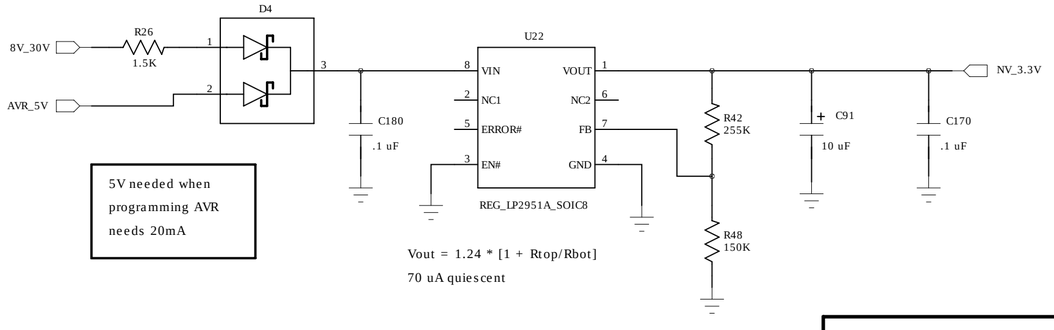
Micro SD Card Socket



5 Channel 12-bit A/D

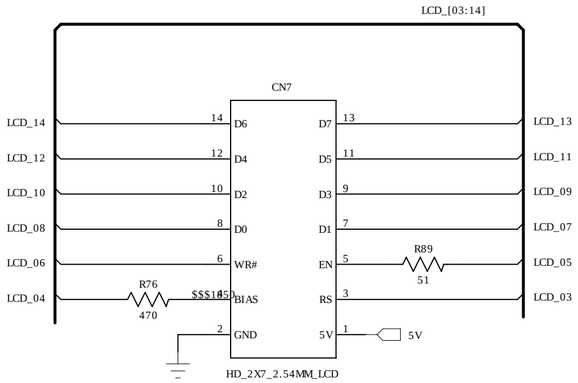


NV 3.3V Regulator for AVR



Technologic Systems		Date July 23, 2015
Title: TS-7800 AVR, SD Card		
Rev: G	Designer	Sheet 10 of 12

LCD Port

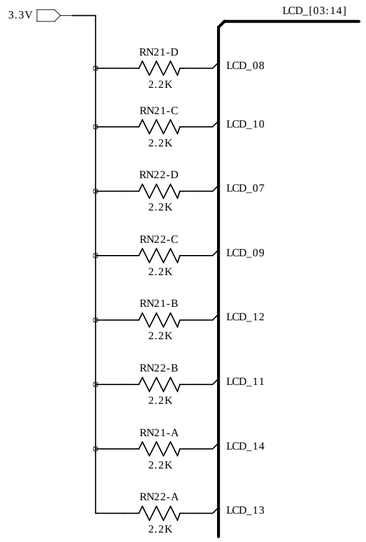


LCD03, LCD05, LCD06 init to inputs
when outputs, active high-low
These are programmable I/O

LCD07 thru LCD14 are always open drain outputs, initialized to high
They can be used as inputs

LCD04 is always output
active high-low, init to zero

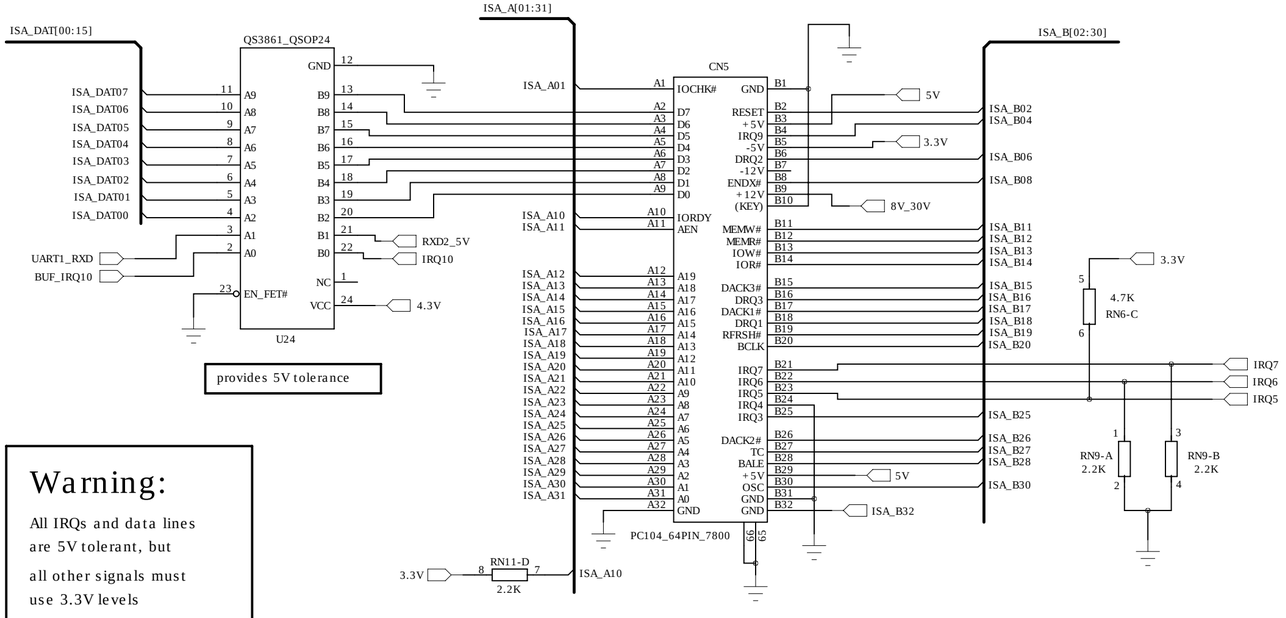
All LCD lines are 5V tolerant



Pull-up resistors for
the open drain outputs

Open drain outputs can
sink 8 mA, but only source
current thru resistor

PC/104 64-pin Connector



provides 5V tolerance

51 lines directly into FPGA
plus 3 more into CPLD (read only)
(IRQ6, IRQ7 and ISA_32)

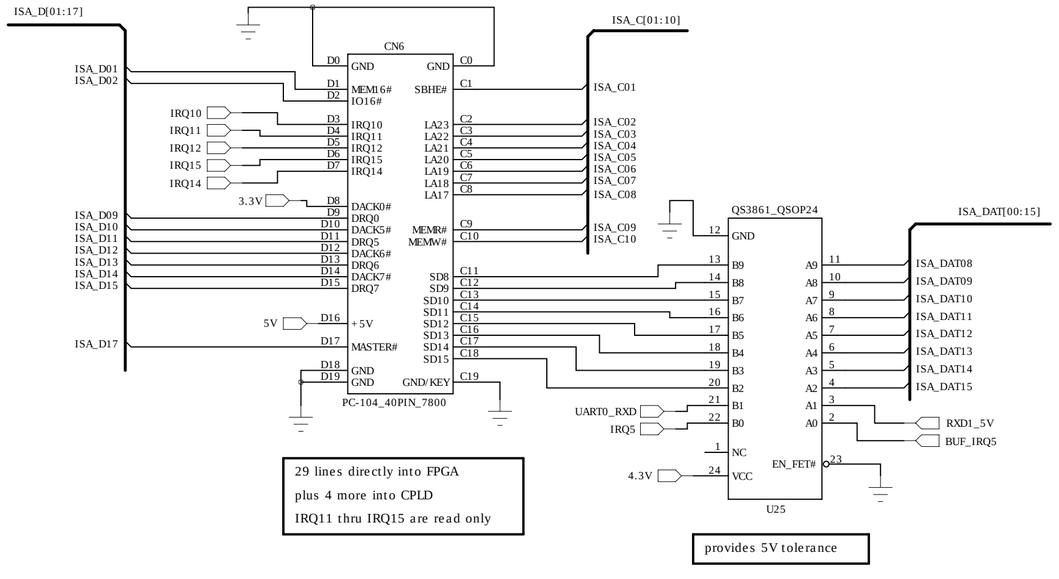
Warning:

All IRQs and data lines
are 5V tolerant, but

all other signals must
use 3.3V levels

IRQ3 must be 3.3V levels

PC/104 40-pin Connector



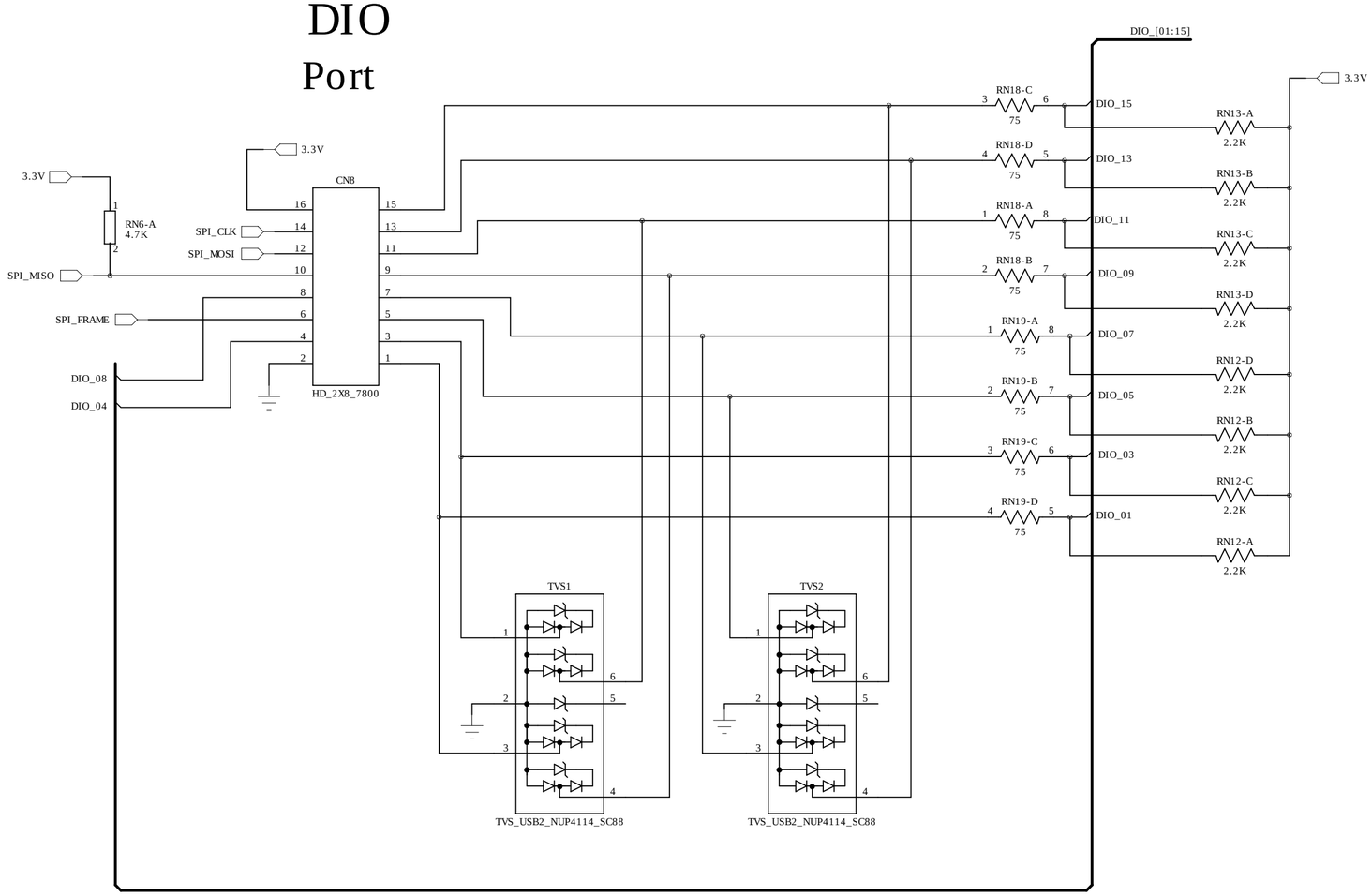
29 lines directly into FPGA
plus 4 more into CPLD
IRQ11 thru IRQ15 are read only

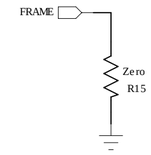
provides 5V tolerance

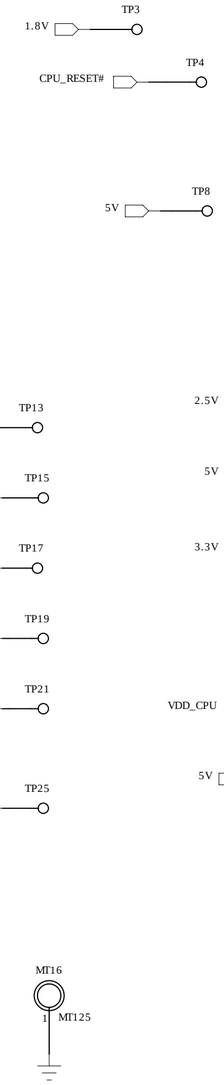
PC/104 40-pin Connector

Technologic Systems	Date July 23, 2015	
Title: TS-7800 DIO, LCD, PC/104		
Rev: G	Designer	Sheet 11 of 12

DIO
Port







SPI_MISO is 5V tolerant
MOSI, CLK, and Frame
are 3.3V level outputs

DIO_01 thru DIO_15 (odds) are always
open drain outputs, initialized to high
They can be used as inputs

DIO_08 initializes to an input
when output, active high-low
It is programmable In or out

DIO_04 is always input
AVR drives pull-up on this pin

Pull-up resistors for
the open drain outputs

Open drain outputs can
sink 8 mA, but only source
current thru resistor

All DIO lines are 5V tolerant

Technologic Systems		Date July 23, 2015
Title: TS-7800 Misc		
Rev: G	Designer	Sheet 12 of 12