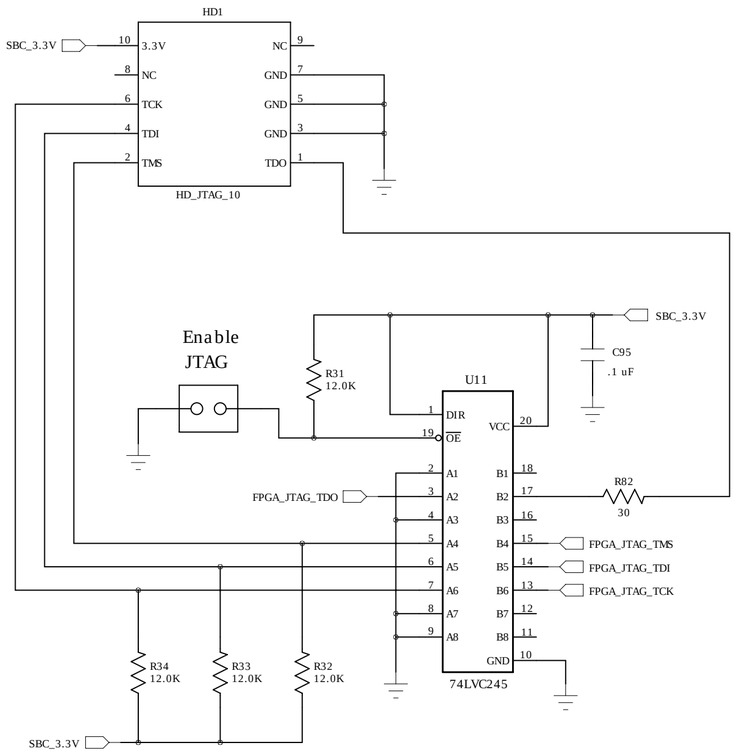
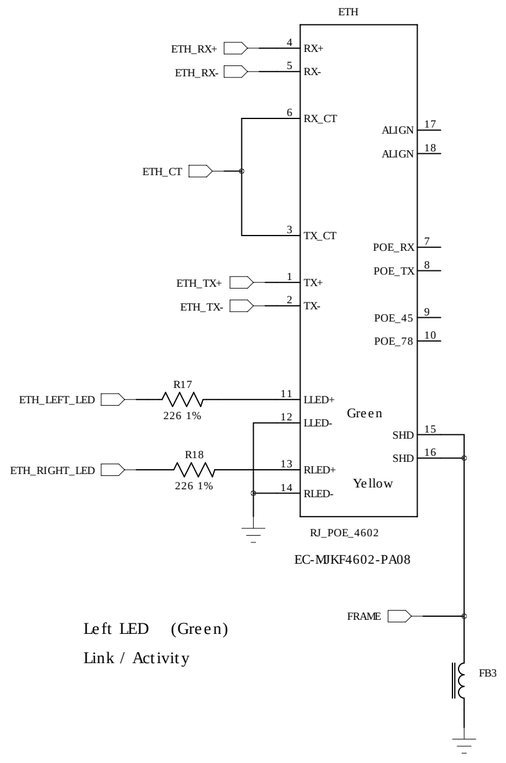
TS-8500

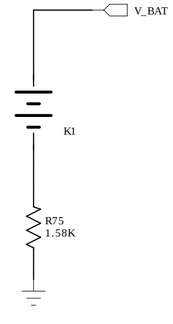
FPGA JTAG Header



10/100 Ethernet

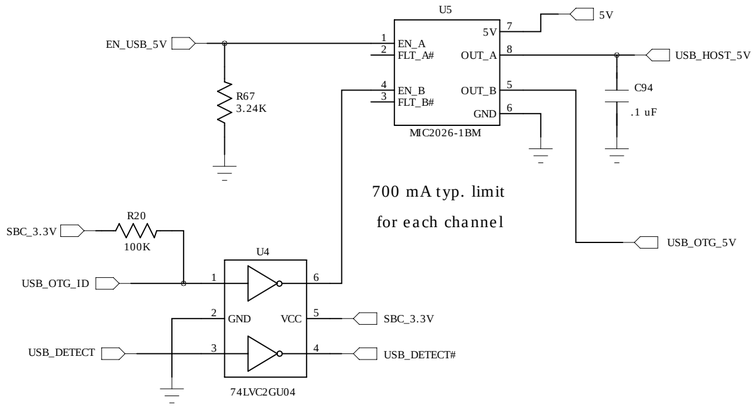


RTC Battery

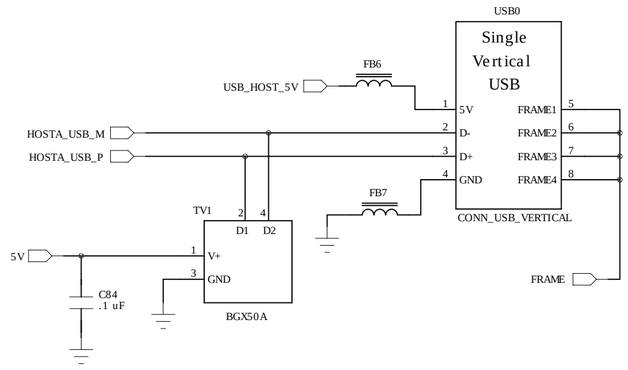


Technologic Systems	Date Aug. 5, 2010	
Title: TS-8500 Ethernet, FPGA JTAG, Battery		
Rev:	Designer	Sheet 1 of 7

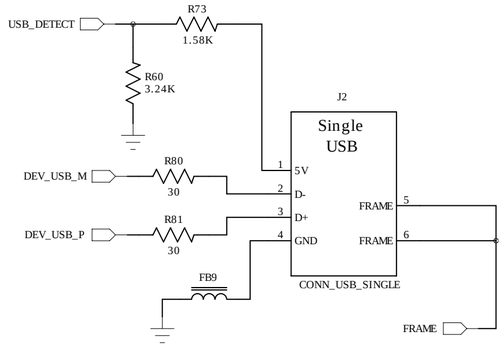
USB Power Switch



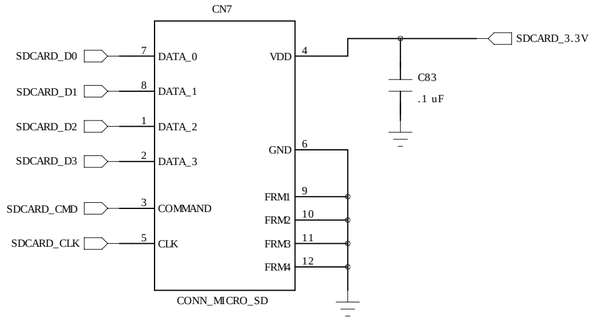
Host USB



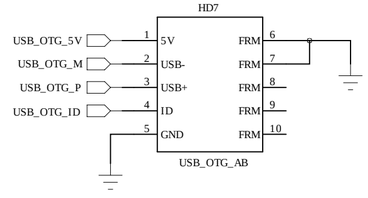
USB Device



Micro SD Card Socket



USB Micro A/B OTG Port

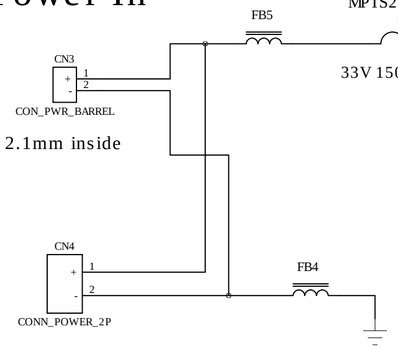


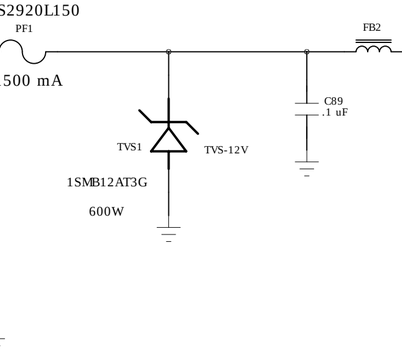
Molex 47590-0001
or 47589-0001

Technologic Systems		Date Aug. 5, 2010
Title: TS-8500 USB, SD socket		
Rev:	Designer	Sheet 2 of 7

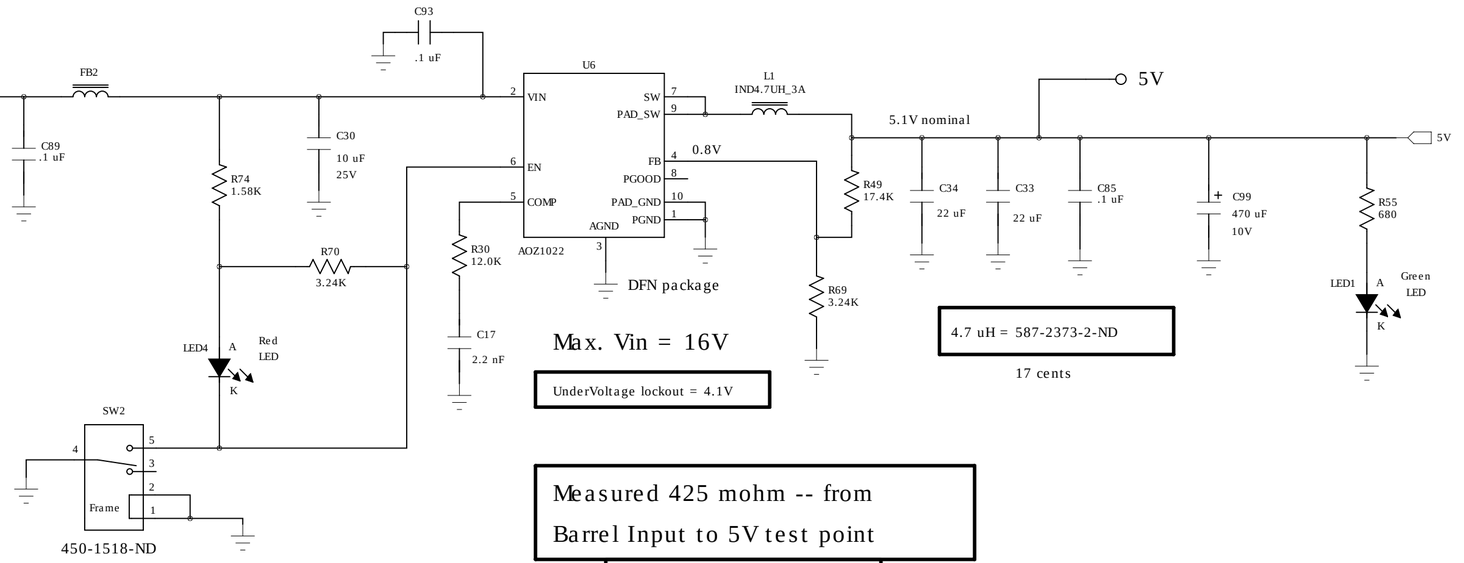
5V to 12V

Power In





5V Regulator



Max. Vin = 16V

UnderVoltage lockout = 4.1V

4.7 uH = 587-2373-2-ND

17 cents

Power Switch

Measured 425 mohm -- from
Barrel Input to 5V test point

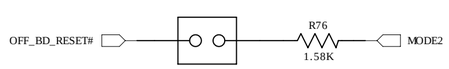
with 5.0V at Input

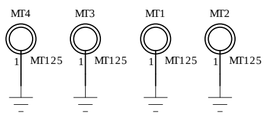
PolyFuse	mohms
1500 mA 33V	122

Ferrite beads = 32 mohm

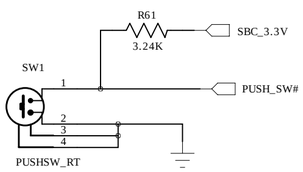
Force Boot to SD card

En. SD
Boot

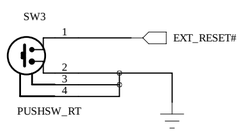




Push Switch



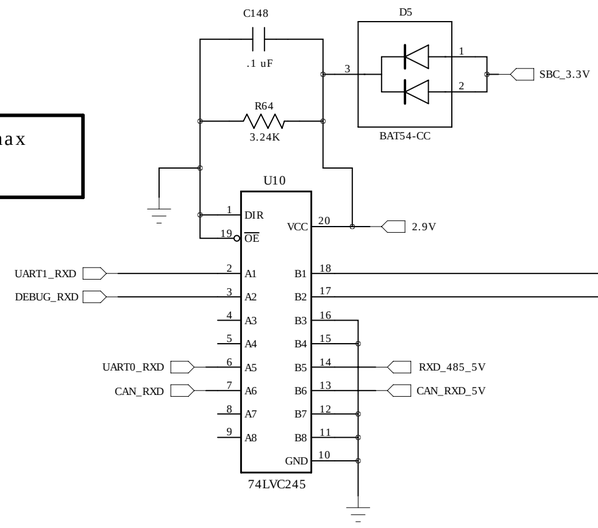
Reset Switch



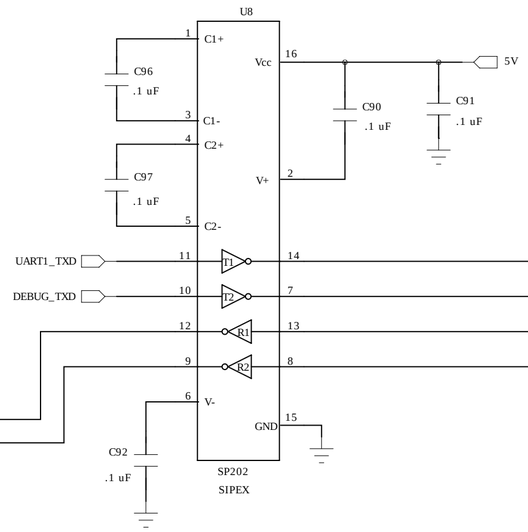
Technologic Systems	Date Aug. 5, 2010	
Title: TS-8500 Power IN, Push Sw. Jumpers		
Rev:	Designer RLM	Sheet 3 of 7

2.9V <-- 5V Level shifter

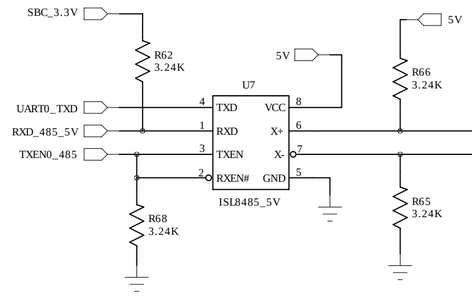
MX515 requires 3.0V max on the RXD pins



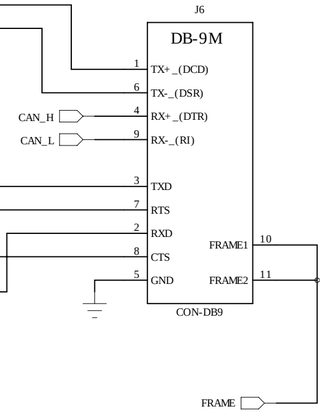
RS-232 Transceiver



RS-485 Driver

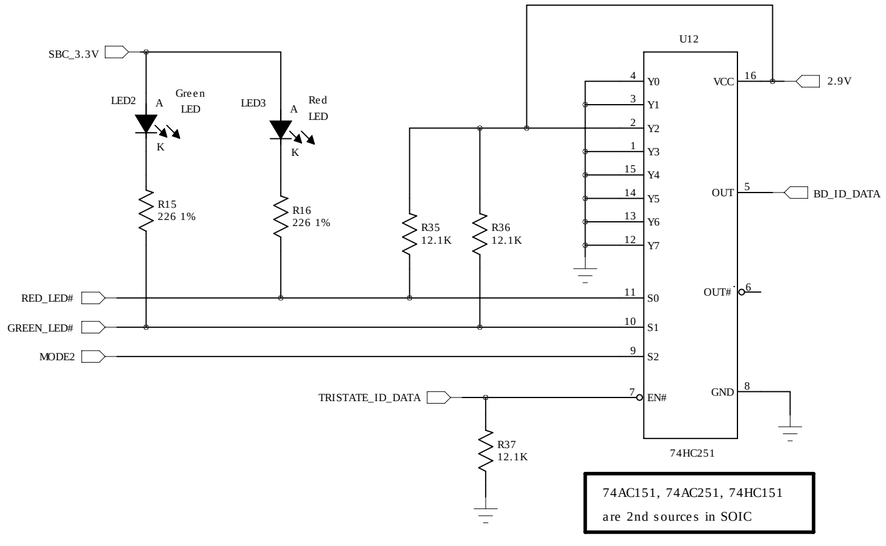


COM DB9M



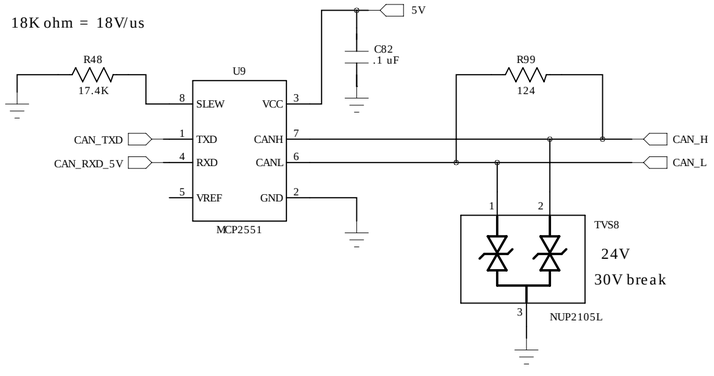
Red and Green LEDs

Board ID = 4



74AC151, 74AC251, 74HC151 are 2nd sources in SOIC

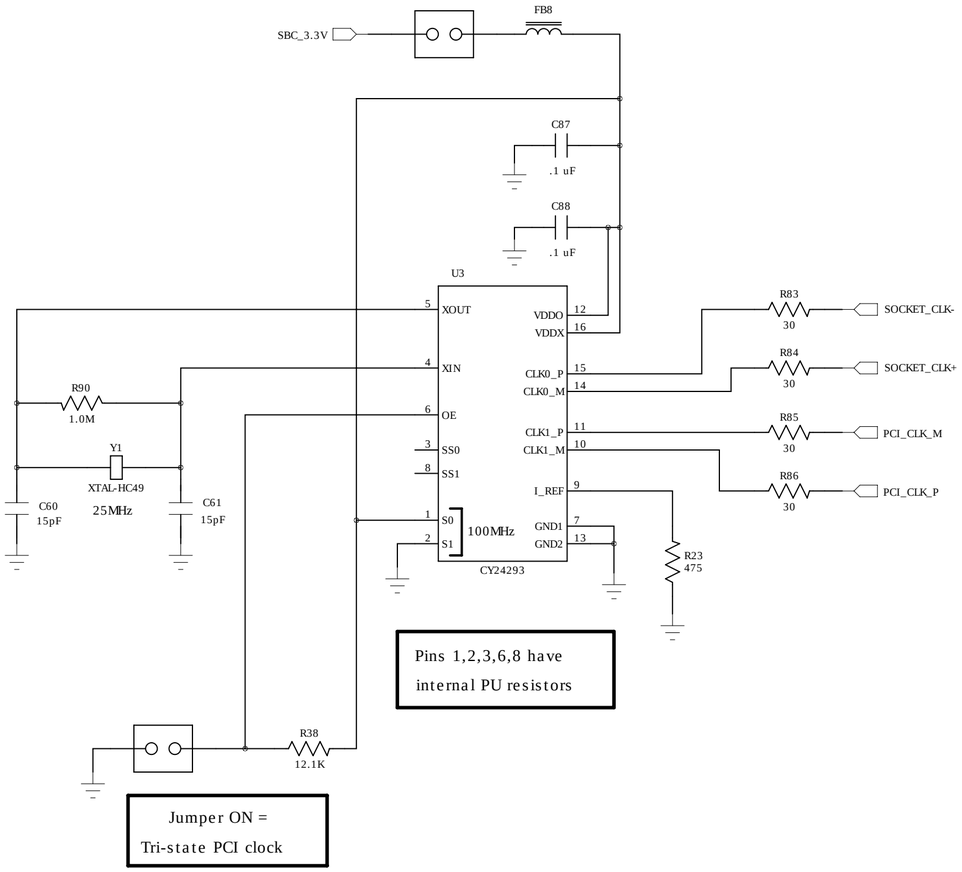
CAN Tranceiver



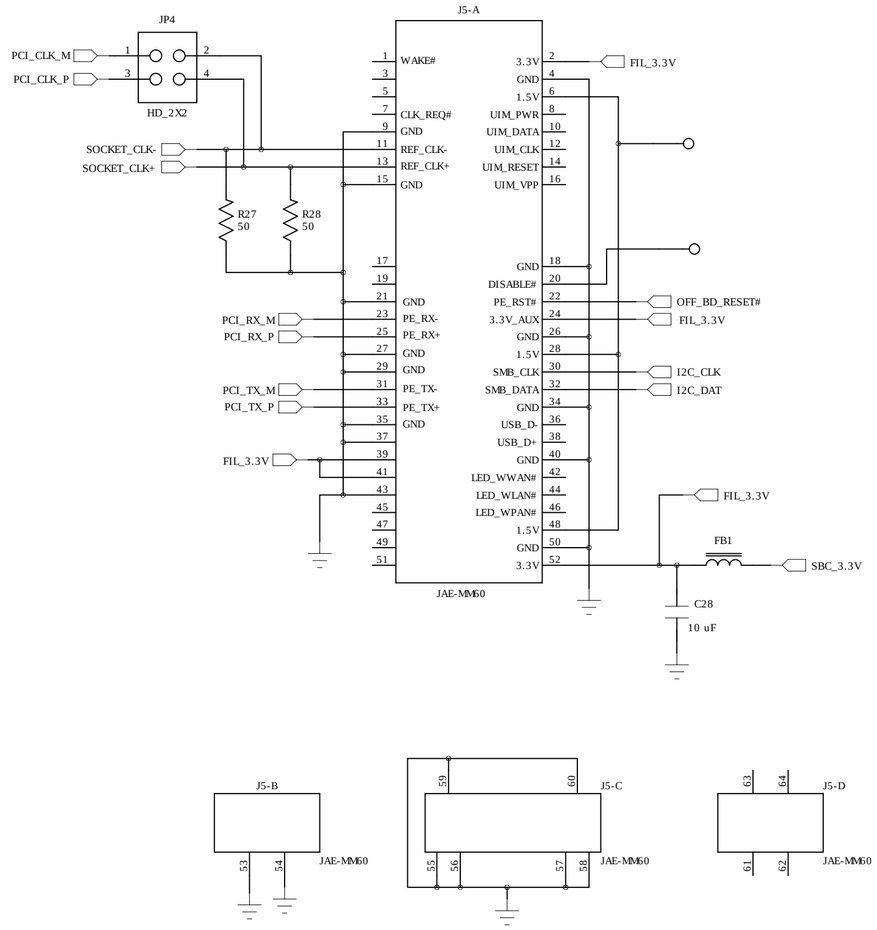
Technologic Systems		Date Aug. 5, 2010
Title: TS-8500 COM port, CAN, RS-485		
Rev:	Designer RLM	Sheet 4 of 7

TS-8210

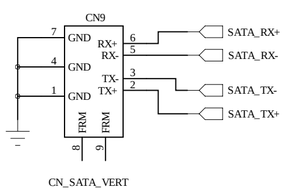
Enable PCIe Clock Power



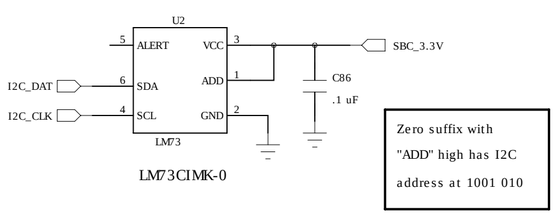
Mini PCIe Socket



SATA Port

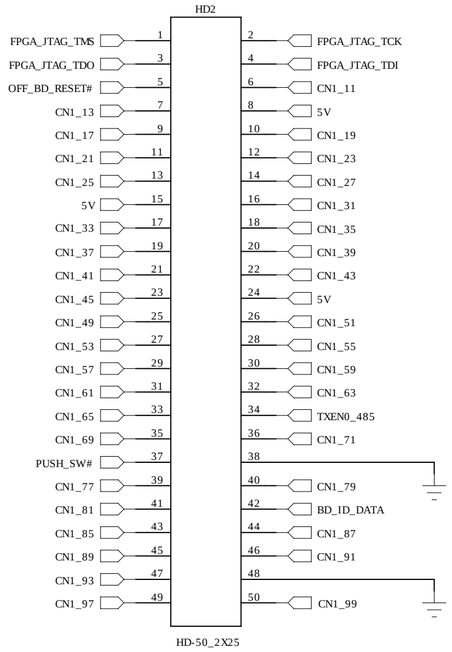


Temp Sensor



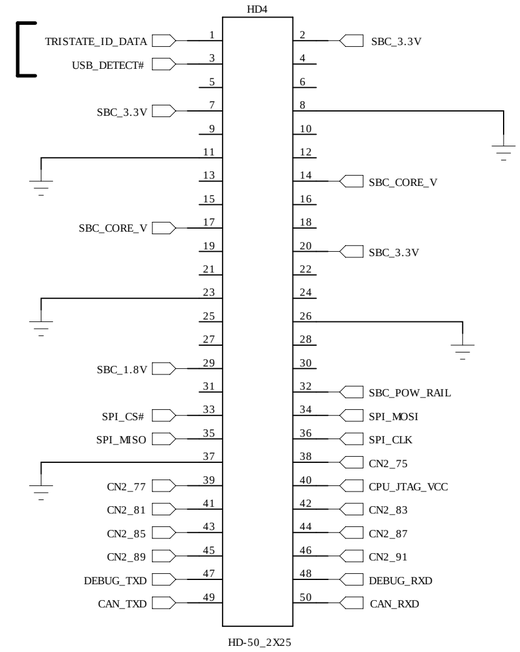
Technologic Systems	Date Aug. 5, 2010	
Title: TS-8500 PCIe and SATA		
Rev:	Designer RLM	Sheet 5 of 7

CN1 Odd Pins



CN2 Odd Pins

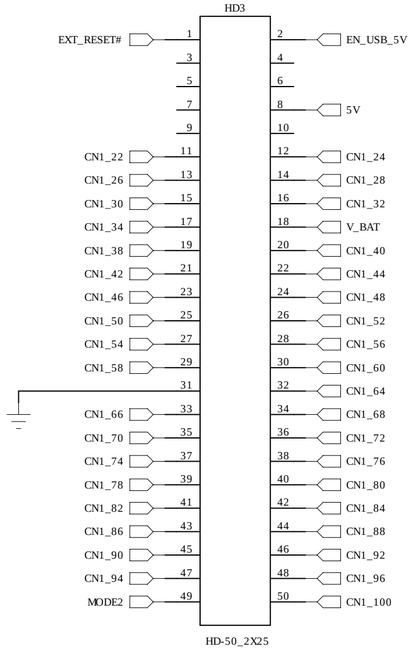
Special signals
Not on CN2



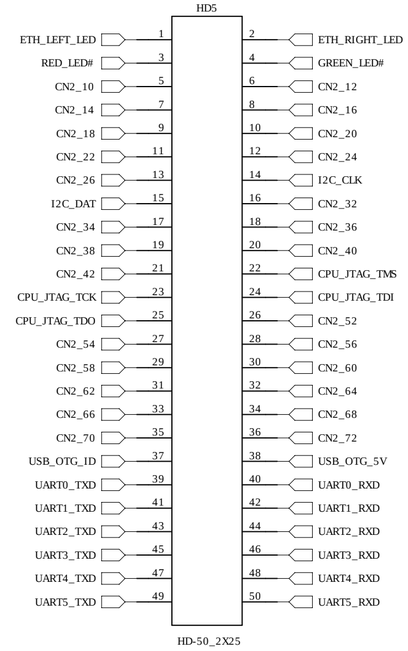
High-speed differential pairs are not routed to these headers

USB, SATA, Ethernet, SD card, PCIe and Ethernet pairs are not connected because this would mismatch the transmission lines.

CN1 Even Pins



CN2 Even Pins



Technologic Systems	Date Aug. 5, 2010	
Title: TS-8500 Headers for SBC signals		
Rev: P1	Designer	Sheet 6 of 7

Two 100-pin Module Connectors

"5V" pins supply all power to the module
Apply 4.5V to 5.5V to these pins

Current drain is < 600 mA
(less than 3 Watts)

EXT_RESET# is an Input to the SBC used to reboot the CPU

Do not drive active high
(use open drain)

Left

CN1

FPGA JTAG: FPGA_JTAG_TMS 1, FPGA_JTAG_TCK 3, FPGA_JTAG_TDO 5, FPGA_JTAG_TDI 7

OFF_BD_RESET# 9

OFF_BD_RESET# is an output from the SBC

5V 15, 5V 29, 5V 47

SD Card: SDCARD_D2 6, SDCARD_D3 8, SDCARD_CMD 10, SDCARD_3.3V 12, SDCARD_CLK 14, 5V 16, SDCARD_D0 18, SDCARD_D1 20

SD card signals on connector are wired in parallel with SD card socket. Only one can be populated with SD card

V_BAT 36

TXEN0_485 67

PUSH_SW# 73

BD_ID_DATA 83

FPGA DIO: CN1_11 11, CN1_13 13, CN1_17 17, CN1_19 19, CN1_21 21, CN1_23 23, CN1_25 25, CN1_27 27, CN1_31 31, CN1_33 33, CN1_35 35, CN1_37 37, CN1_39 39, CN1_41 41, CN1_43 43, CN1_45 45, CN1_49 49, CN1_51 51, CN1_53 53, CN1_55 55, CN1_57 57, CN1_59 59, CN1_61 61, CN1_63 63, CN1_65 65, CN1_69 69, CN1_71 71, CN1_77 77, CN1_79 79, CN1_81 81, CN1_85 85, CN1_87 87, CN1_89 89, CN1_91 91, CN1_93 93, CN1_97 97, CN1_99 99

FPGA DIO: CN1_22 22, CN1_24 24, CN1_26 26, CN1_28 28, CN1_30 30, CN1_32 32, CN1_34 34, CN1_38 38, CN1_40 40, CN1_42 42, CN1_44 44, CN1_46 46, CN1_48 48, CN1_50 50, CN1_52 52, CN1_54 54, CN1_56 56, CN1_58 58, CN1_60 60, CN1_64 64, CN1_66 66, CN1_68 68, CN1_70 70, CN1_72 72, CN1_74 74, CN1_76 76, CN1_78 78, CN1_80 80, CN1_82 82, CN1_84 84, CN1_86 86, CN1_88 88, CN1_90 90, CN1_92 92, CN1_94 94, CN1_96 96, CN1_100 100

MODE2 98

CON100_5179029-4_TYCO

Right

CN2

Ethernet: ETH_RX+ 1, ETH_RX- 3, ETH_CT 5, ETH_TX+ 7, ETH_TX- 9, ETH_CT 11

Maximum load on 3.3V pin is 500 mA

SBC_3.3V 13, SBC_3.3V 39

SATA_RX- 17, SATA_RX+ 19

DEV_USB_M 23, DEV_USB_P 25

SBC_CORE_V 27

C81 .1 uF

HOSTA_USB_M 29, HOSTA_USB_P 31

USB_OTG_M 35, USB_OTG_P 37

SATA_TX- 41, SATA_TX+ 43

PCI_TX_M 47, PCI_TX_P 49

PCI_RX_M 53, PCI_RX_P 55

SBC_1.8V 57

PCI_CLK_M 59, PCI_CLK_P 61

SBC_POW_RAIL 63

SPI Bus: SPI_CS# 65, SPI_MOSI 67, SPI_MISO 69, SPI_CLK 71

CN2_75 75, CN2_77 77

CPU_JTAG_VCC 79

CN2_81 81, CN2_83 83, CN2_85 85, CN2_87 87, CN2_89 89, CN2_91 91

Console: DEBUG_TXD 93, DEBUG_RXD 95

CAN: CAN_TXD 97, CAN_RXD 99

ETH_LEFT_LED 2, ETH_RIGHT_LED 4, RED_LED# 6, GREEN_LED# 8

CN2_10 10, CN2_12 12, CN2_14 14, CN2_16 16, CN2_18 18, CN2_20 20, CN2_22 22, CN2_24 24, CN2_26 26

I2C: I2C_CLK 28, I2C_DAT 30

CN2_32 32, CN2_34 34, CN2_36 36, CN2_38 38, CN2_40 40, CN2_42 42

CPU JTAG: CPU_JTAG_TMS 44, CPU_JTAG_TCK 46, CPU_JTAG_TDI 48, CPU_JTAG_TDO 50

CN2_52 52, CN2_54 54, CN2_56 56, CN2_58 58, CN2_60 60, CN2_62 62, CN2_64 64, CN2_66 66, CN2_68 68, CN2_70 70, CN2_72 72

USB_OTG_ID 74, USB_OTG_5V 76

Serial Ports or DIO: UART0_TXD 78, UART0_RXD 80, UART1_TXD 82, UART1_RXD 84, UART2_TXD 86, UART2_RXD 88, UART3_TXD 90, UART3_RXD 92, UART4_TXD 94, UART4_RXD 96, UART5_TXD 98, UART5_RXD 100

CON100_5179029-4_TYCO

Mode 2	Boots from
1	NAND Flash
0	SD Card

MODE2 state is latched prior to OFF_BD_RESET# deasserted

MODE2 has a 12K PU on the SBC module

Use 1.5K ohm resistor to GND to set low

Technologic Systems	Date Aug. 5, 2010	
Title: TS-8500 Dual 100-pin Module Connectors		
Rev:	Designer RLM	Sheet 6 of 7